VISVESVARAYA TECHNOLOGICAL UNIVERSITY

JNANA SANGAMA, BELGAVI -590 014

Study Materials

Electronics Principals Circuites (BEC303)

(IPCC)

(Effective from the academic Year 2025-2026)

SEMESTER – III

Subject Code: BEC303

(Choice Based Credit System)

Prepared by:	HOD
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Department Of Information Science and Engineering

Akshaya Institute of Technology

(Affiliated to VTU, Belgum& Approved by AICTE, New Delhi)

Lingapura,Obalapura Post, Koratagere Road,Tumakuru-572106

Akshaya Institute of Technology

(Recognized by AICTE, New Delhi and Affiliated to Visvesvaraya Technological , University, Belagavi)
Akshaya Institute of Technology lingapura, Obalapura post, Koratagere Road, Tumakuru-distric-572106, Karnataka State, INDIA.

Year: 2025 - 2026

Electronics Principals Circuites (BEC303)

(IPCCBEC303)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Effective from the academic Year 2025-26)
SEMESTER – III
Subject Code: BEC303
(Choice Based Credit System)

STUDENT'S NAME: ……

USN: ……

BRANCH: ……

SECTION: …… **YEAR:** ……

Vision

To produce competent engineering professionals in the field of Electronics & Communincations Engineering by imparting value based quality technical education to meetthe societal needs and develop socially responsible citizens

Mission

M1: To provide strong fundamentals and technical skills in the field of Electronics and communication Engineering through effective teaching learning process.

M2: Enhancing employ ability of the students by providing skills in the fields of VLSI, Embedded systems

M3: Encourage the students to participate in co curricular and extra curricular activities that creates a spirit of social responsibility and leadership qualities.

Program Outcomes

Sl. No.	Description	POs
1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and computer science and business systems to the solution of complex engineering and societal problems.	PO1
2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering and business problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	PO2
3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	PO3
4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	PO4
5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations	PO5
6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering and business practices.	PO6
7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in business societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	PO7
8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering and business practices.	PO8
9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	PO9
10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	PO10
11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering, business and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	PO11
12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	PO12

Electronic Principles and Circuits		Semester	3
Course Code	**BEC303**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3
Examination nature (SEE)	Theory/Practical		

Course objectives:

This course will enable students to

- Design and analyse the BJT circuits as an amplifier and voltage regulation.
- Design of MOSFET Amplifiers and analyse the basic amplifier configurations using small signal equivalent circuit models
- Design of operational amplifiers circuits as Comparators, DAC and filters.
- Understand the concept of positive and negative feedback.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.
- Understand the thyristor operation and the different types of thyristors.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4.Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

MODULE-1

BJT AC models: Base Biased Amplifier, Emitter Biased Amplifier, Small Signal Operation, AC Beta, AC Resistance of the emitter diode, Two transistor models, Analyzing an amplifier.

Voltage Amplifiers: Voltage gain, Multistage Amplifiers.

CC and CB Amplifiers: CC Amplifier, Output Impedance, Cascading CE and CC, Darlington Connections, Voltage regulation, The Common base Amplifier.

[Text1]

MODULE-2

MOSFET

Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modelling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance, The Common Gate Amplifier, Source follower.

MODULE-3

Linear Opamp Circuits: Summing Amplifier and D/A Converter, Nonlinear Op-amp Circuits: Comparator with zero reference, Comparator with non-zero references. Comparator with Hysteresis.

Oscillator: Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator.

The 555 timer: Monostable Operation, Astable Operation.

[Text1]

MODULE-4

Negative Feedback: Four Types of Negative Feedback, VCVS Voltage gain, Other VCVS Equations, ICVS Amplifier, VCIS Amplifier, ICIS Amplifier (No Mathematical Derivation).

Active Filters: Ideal Responses, First Order Stages, VCVS Unity Gain Second Order Low pass Filters, VCVS Equal Component Low Pass Filters, VCVS High Pass Filters, MFB Bandpass Filters, Bandstop Filters.

[Text1]

MODULE-5

Power Amplifiers: Amplifier terms, Two load lines, Class A Operation, Class B operation, Class B push pull emitter follower, Class C Operation.

Thyristors: The four layer Diode, SCR, SCR Phase control, Bidirectional Thyristors, IGBTs, Other Thyristors.

[Text1]

PRACTICAL COMPONENT OF IPCC *(Experiments can be conducted either using any circuit simulation software or discrete components)*

Sl.NO	Experiments
1	Design and Test (i) Bridge Rectifier with Capacitor Input Filter (ii) Zener voltage regulator
2	Design and Test Biased Clippers – a)Positive, b) Negative , c) Positive-Negative Positive and Negative Clampers with and without Reference.
3	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.
4	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.
5	Design and test (i) Emitter Follower , (ii) Darlington Connection
6	Design and plot the frequency response of Common Source JFET/MOSFET amplifier
7	Test the Opamp Comparator with zero and non zero reference and obtain the Hysteresis curve.
8	Design and test Full wave Controlled rectifier using RC triggering circuit.
9	Design and test Precision Half wave and full wave rectifiers using Opamp
10	Design and test RC phase shift oscillator

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits.
2. Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions.
3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.
4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.
5. Understand the power electronic device components and its functions for basic power electronic circuits.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Books

1. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017, ISBN:978-0-07-063424-4.
2. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6thEdition, Oxford, 2015.ISBN:978-0-19-808913-1

Web links and Video Lectures (e-Resources):

1. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
2. Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Electronic Principles and Circuits

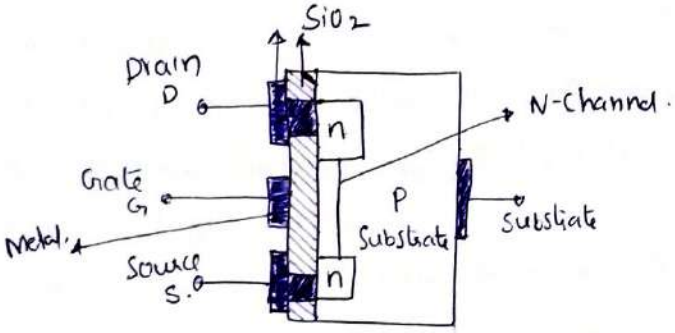
Module - 2

MOSFET

* Metal Oxide Semiconductor Field Effect Transistor.
* Here Gate terminal is insulated from channel by a SiO_2 layer. Due to this input resistance is high.
* Because of insulated Gate, it is called IGFET.
* There are two types of MOSFET a) Depletion MOSFET
  b) Enhancement MOSFET

Depletion MOSFET

→ The structure of N-channel Depletion MOSFET is given by

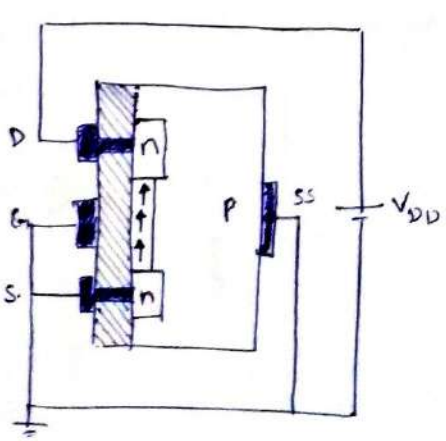


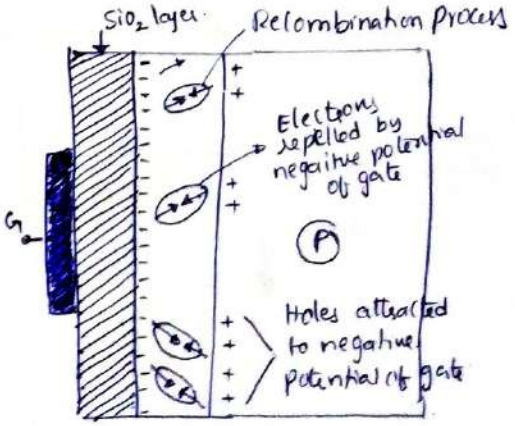
→ Two specially doped n regions are diffused with a lightly doped p-type substrate. These doped 'n' regions form source and Drain.

→ The source and drain terminals are linked through metallic bond to n-doped regions attached through n-channel.

→ The Gate is also connected to a metal contact surface but it stays insulated from n-channel by a very thin layer of SiO_2.

→ There is no direct electrical connection between Gate and channel of MOSFET, increasing the input impedance of device.





→ When V_{DS} is applied keeping $V_{GS}=0$ by directly connecting gate to source terminal, free electrons from the n-channel are attracted towards positive potential of drain terminal.

→ This establishes current through the channel to be noted as I_{DSS} at $V_{GS}=0$.

→ Apply negative gate voltage, then the negative charges on the gate repel conduction electrons from channel and attract holes from P-substrate.

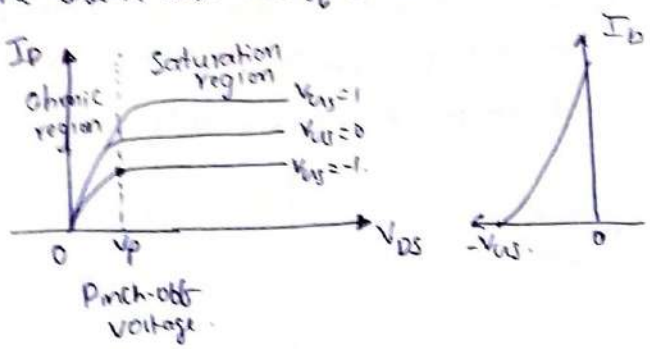
→ This initiates recombination of repelled electrons and attract holes. Electrons and holes recombination depends on the magnitude of negative voltage applied to gate.

→ Number of free electrons reduced due to this recombination in n-channel for the conduction, reducing drain current.

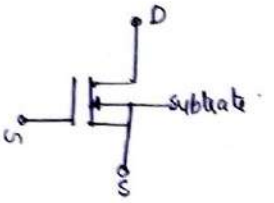
→ The n-channel is depleted some of its electrons thus decreasing the channel conductivity because of recombination.

→ With increasing negative bias for V_{GS} the level of drain current will get reduced.

→ The drain and transfer characteristics are given by.

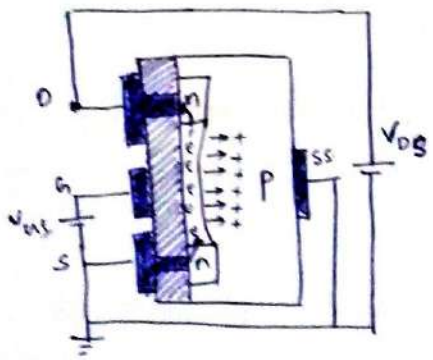


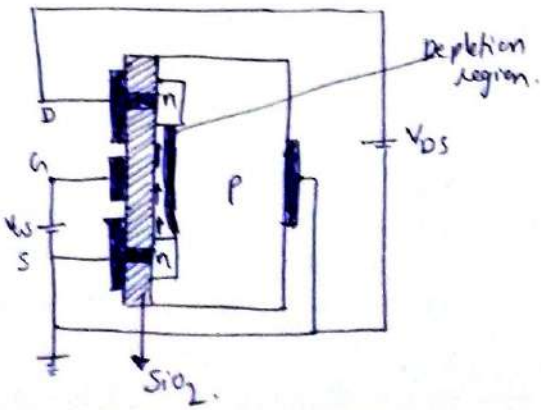
The symbol of n channel D-MOSFET is given as



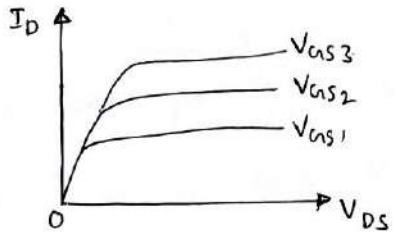
Enhancement MOSFET

Two highly doped n regions are diffused into a lightly doped P-type substrate. The source and drain are taken out through metallic contacts to n-doped region. The channel formation in MOSFET is shown as.

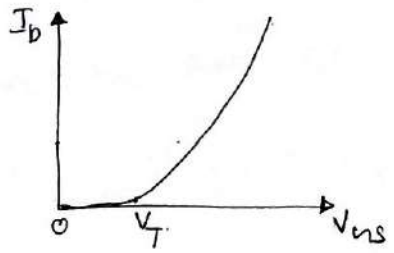




* The SiO_2 layer is to isolate the gate metallic platform from the region between the drain and source.
* When a positive voltage V_{GS} is applied between the gate and source terminal, the gate attracts the minority carriers ie electrons from P-type substrate.
* These electrons accumulate near the surface of SiO_2 layer thereby inducing n-channel. The holes present in p-substrate get repelled from the edge of SiO_2 layer and move away deep into P-substrate.
* The SiO_2 layer acts as a strong barrier and prevents the electrons in the induced channel from being attracted by gate terminal.
* The drain current I_D now flows through the induced channel due to flow of those accumulated electrons.
* As V_{GS} is increased more and more electrons accumulate in the induced channel leading to enhanced flow of drain current.
* The lowest value of V_{GS} that just leads to the flow of drain current is referred as Threshold voltage V_t.
* As the channel does not exist with $V_{GS}=0$ and enhanced due to the application of a positive gate to source voltage. Hence this type of MOSFET is called Enhancement MOSFET.
* The drain characteristics are given by.



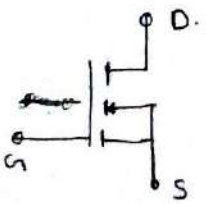
* The transfer characteristics are given by.



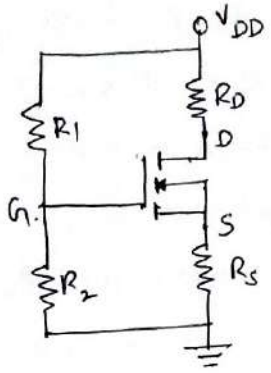
For $V_{GS} > V_T$ the relationship between drain current and V_{GS} is non linear and it is given as

$$I_D = K (V_{GS} - V_T)^2.$$

* The Symbol of n-channel Enhancement MOSFET is



Voltage Divider Bias of n-channel Enhancement MOSFET



The voltage divider circuit consists of resistor R_1 and R_2 to provide positive gate to source voltage.

For DC analysis Gate current $I_G = 0$.

$$V_G = \frac{R_2}{R_1 + R_2} \cdot V_{DD}$$

Applying KVL to input part of the circuit.

$$V_G - V_{GS} - V_S = 0$$

$$V_S = I_S R_S$$

$$V_{GS} = V_G - V_S = V_G - I_S R_S$$

But $I_S = I_D$

$$V_{GS} = V_G - I_D R_S$$

$$\boxed{I_D = \frac{V_{GS} - V_G}{R_S}}$$

Applying KVL to output part of the circuit

$$V_{DD} - I_D R_D - V_{DS} - I_S R_S = 0$$

$$I_D = I_S$$

$$V_{DD} - I_D R_D - V_{DS} - I_D R_S = 0$$

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$\boxed{V_{DS} = V_{DD} - I_D (R_D + R_S)}$$

The Drain current of MOSFET is given by

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

μ_n = mobility of electron.

C_{ox} = oxide layer capacitance.

$\frac{W}{L}$ = Aspect ratio.

Biasing in MOS Amplifier Circuit

* The DC operating point is characterized by a stable and predictable dc drain current I_D and by a DC drain to source voltage V_{DS}.
* After fixing the operating point, MOSFET is operated in ohmic region so that it acts as an Amplifier.
* During the operation of amplifier, the operating point is to be kept constant by the cause of any disturbances.
* To keep the operating point as constant, we have to adopt techniques.

a) Biasing by Fixing V_{GS}

→ Here the Gate to source voltage V_{GS} is kept constant to provide I_D. This V_{GS} is derived from V_{DD} through the voltage divider.

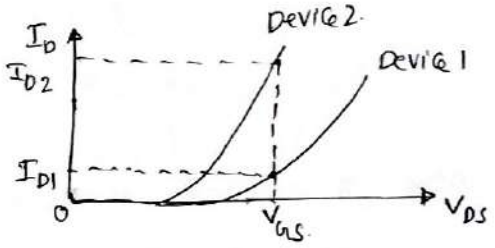
→ The current equation is given by

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

Here μ_n, C_{ox}, $\frac{W}{L}$ and V_t are constant values.

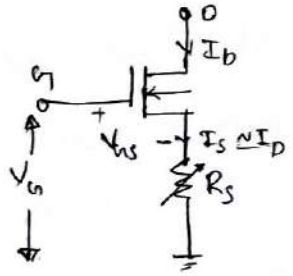
→ By fixing V_{GS} also constant, we can maintain constant I_D value. Once I_D maintained constant V_{DS} also kept constant.

→ The use of fixed bias can result in a large variability in the value of I_D.



b) Biasing by Fixing V_G and Connecting a source resistance.

→ The circuit configuration is given as.



→ It consists of fixing the DC voltage at gate V_G and connecting a resistance at the source terminal.

From Diagram $V_G = V_{GS} + I_D R_S$.

→ By any reason if I_D increases, to keep V_{GS} as constant, V_{GS} is to be decreased

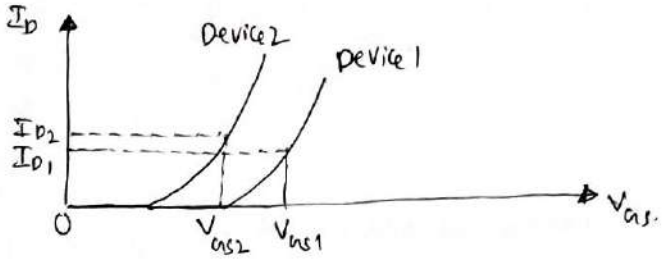
→ If V_{GS} decreases, I_D is decreased using the current equation

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$$

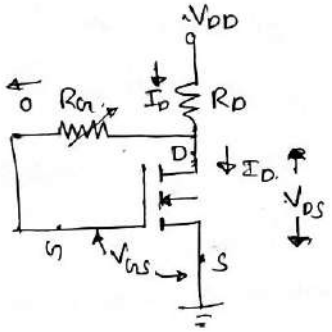
→ To keep V_{GS} as constant V_{GS} is increased, if V_{GS} increases, I_D is again increases. This process continues.

→ The variable source resistance 'R_S' will keep the I_D value constant. So the above process cannot happens. This resistance is also called as degeneration resistance.

→ The transfer characteristics for two devices is given as.



c) Biasing using a Drain to Gate Feedback Resistor



→ Here the large feedback resistance R_G forces the DC voltage at the gate to be equal to that of drain.

The gate current $I_G = 0$ due to high R_G

$$V_{GS} = V_{DS} = V_{DD} - I_D R_D.$$

$$V_{DD} = V_{GS} + R_D I_D$$

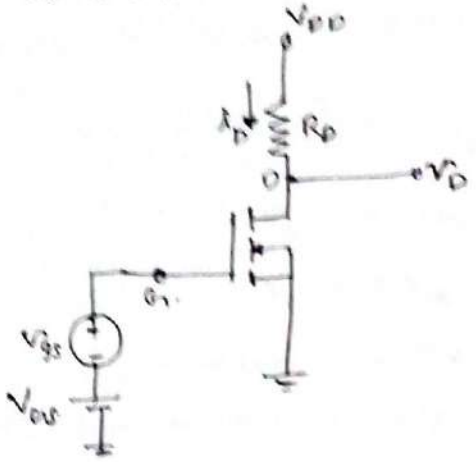
→ If I_D increases, V_{GS} must decrease to maintain V_{DD} constant. The decrease in V_{GS} in turn causes a decrease in I_D.

→ If I_D decreases, V_{GS} must increase. The increase in V_{GS} in turn causes an increase in I_D. This continues.

→ The resistance R_G will keep the value of I_D as constant., so V_{DS} also maintains constant.

Small Signal Operation of MOSFET

We are using common source Amplifier. Here MOSFET is biased by applying a DC Voltage V_{GS}. The input signal to be amplified is v_{gs} is superimposed on the DC bias voltage V_{GS}. The output voltage is taken at the Drain.



The DC Bias point

* The DC bias current I_D can be finded by setting the signal v_{gs} to Zero.

$$I_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2$$

* The DC voltage at the drain V_{DS} or V_D will be.

$$V_D = V_{DD} - R_D I_D$$

* To obtain Saturation region operation, the condition is

$$V_D > V_{GS} - V_t$$

* The overdrive voltage is given as $V_{OV} = V_{GS} - V_t$.

The Signal Current in the Drain terminal

* The input signal v_{gs} is applied at Gate terminal. The total instantaneous gate to soure voltage will be.

$$V_{gs} = V_{GS} + v_{gs}$$

* The instantaneous drain current i_d is

$$I_d = \frac{1}{2} K_n' \frac{W}{L} (V_{gs} - V_t)^2$$

$$= \frac{1}{2} K_n' \frac{W}{L} (V_{GS} + v_{gs} - V_t)^2$$

$$= \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t + v_{gs})^2$$

$$I_d = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2 + K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs} + \frac{1}{2} K_n' \frac{W}{L} v_{gs}^2$$

① ② ③

* The first term is DC bias current I_D ; The second term is a current component that is directly proportion to the input signal v_{gs} The third term is a current component that is proportional to the square of the input signal.

* The last component is not desirable because it represents non Linear distortion.. To reduce this distortion, the input signal should be kept small.

$$\frac{1}{2} K_n' \frac{W}{L} v_{gs}^2 < K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}$$

$$v_{gs} < 2 (V_{GS} - V_t)$$

$$v_{gs} < 2 V_{OV}$$

V_{OV} is overdrive voltage.

* If this small signal condition is satisfied, last term is neglected. So

$$I_d = I_D + i_d.$$

$$i_d = K_n' \frac{W}{L} (V_{GS} - V_t) v_{gs}.$$

Transconductance $g_m = \frac{i_d}{v_{gs}} = K_n' \frac{W}{L} (V_{GS} - V_t)$

$$\boxed{g_m = K_n' \frac{W}{L} V_{OV}}$$

Voltage gain

The total instantaneous drain voltage v_d is given as.

$$v_d = V_{DD} - R_D I_d.$$

$$= V_{DD} - R_D (I_D + i_d).$$

$$v_d = \underbrace{V_{DD} - R_D I_D}_{V_D} \underbrace{- R_D i_d}_{v_d}.$$

$$v_d = V_D + R_D i_d.$$

So the drain voltage is given by

$$v_d = -i_d R_D.$$

$$= - g_m v_{gs} R_D.$$

Voltage gain A_V is given by

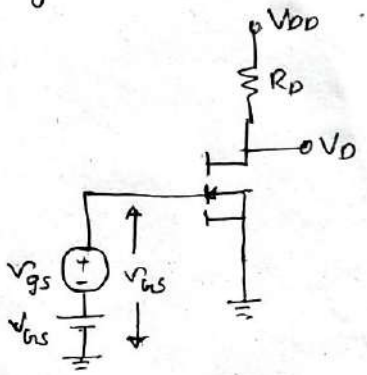
$$A_V = \frac{v_d}{v_{gs}} = \frac{- g_m v_{gs} \cdot R_D}{v_{gs}}.$$

$$\boxed{A_V = - g_m R_D}$$

The output signal v_d is 180° out of phase with respect to input signal v_{gs}.

Small signal operation

The common source amplifier in which MOS transistor is biased by dc voltage V_{GS} is given as.



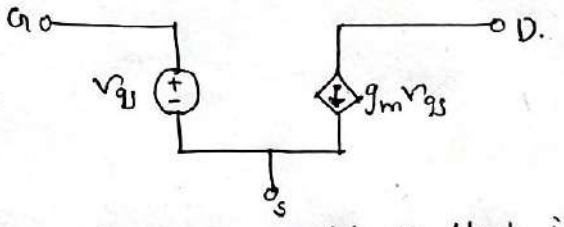
The input signal v_{gs} is super imposed on DC bias voltage V_{GS}. The output signal is taken at drain.

$$I_D = \frac{1}{2} K_n' \frac{W}{L} (V_{GS} - V_t)^2$$

$$V_D = V_{DD} - I_D R_D.$$

Π-model

* FET is a voltage controlled current device. It accepts a signal v_{gs} and provides a current $g_m v_{gs}$ at drain terminal.
* The input resistance is very high and output resistance is also high. Transistor can be replaced by equivalent circuit as.

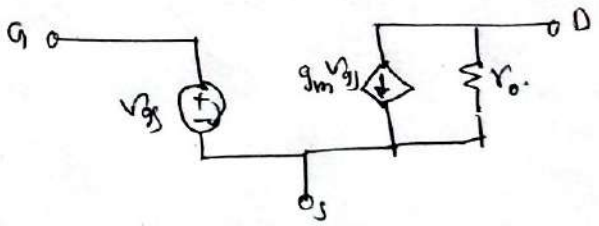


* The problem of above model is that it assumes the drain current in saturation is independent of drain voltage. But in reality drain current does infact depend on V_{DS} in linear manner.
* This dependence was modeled by a finite resistance r_o between drain and source, given as $r_o = \frac{|V_A|}{I_D}$

  where $V_A = \frac{1}{\lambda}$, λ = MOSFET parameter.

  V_A is proportional to Channel length.

* The new Π-model equivalent circuit is



The g_m and r_o generally depend on the DC bias point of MOSFET.

Voltage gain is $A_v = \frac{v_d}{v_{gs}} = -g_m(R_D \parallel r_o)$

Transconductance g_m

The general formula of transconductance is.

$$g_m = k_n' \frac{W}{L}(V_{GS} - V_t) \quad \text{——} ①$$

$$g_m = k_n' \frac{W}{L} V_{OV}.$$

→ g_m is proportional to k_n' and $\frac{W}{L}$, so to obtain the large value of conductance, the transistor must be short and wide.

→ g_m is also proportional to V_{OV}. Increasing of g_m by biasing the device at a bigger value V_{GS} has the disadvantage of reducing the voltage swing at drain

→ From current expression. $I_D = \frac{1}{2} k_n' \frac{W}{L}(V_{GS} - V_t)^2$

we can write $V_{GS} - V_t = \frac{\sqrt{2I_D}}{\sqrt{k_n'\left(\frac{W}{L}\right)}}$

Substituting the value of $V_{GS} - V_t$ in equation ①

$$g_m = k_n' \frac{W}{L} \cdot \frac{\sqrt{2I_D}}{\sqrt{k_n' \frac{W}{L}}} = \sqrt{2k_n' I_D \left(\frac{W}{L}\right)}$$

Here g_m is proportion to the square root of DC bias current.

and also g_m is proportioned to $\sqrt{W/L}$.

→ From current equation we can write again as.

$$k_n'\left(\frac{W}{L}\right) = \frac{2I_D}{(V_{GS} - V_t)^2}$$

Substituting the above value in equation ①.

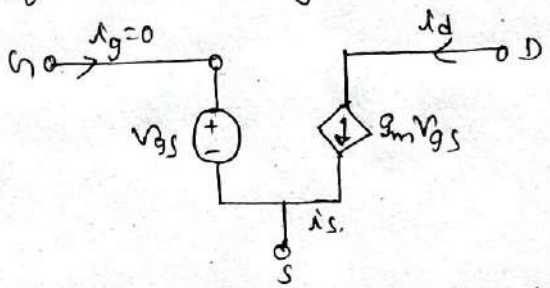
$$g_m = \frac{2I_D}{(V_{GS} - V_t)^2} \cdot (V_{GS} - V_t)$$

$$g_m = \frac{2I_D}{V_{GS} - V_t} = \frac{2I_D}{V_{OV}}.$$

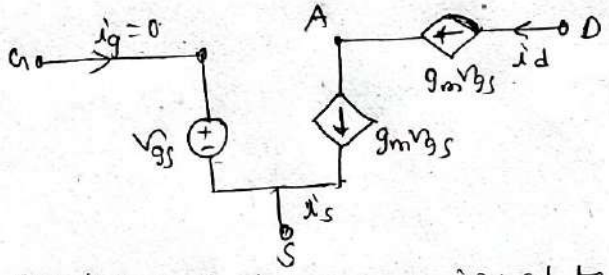
→ So totally g_m has three different equations.

T-equivalent Model of MOSFET

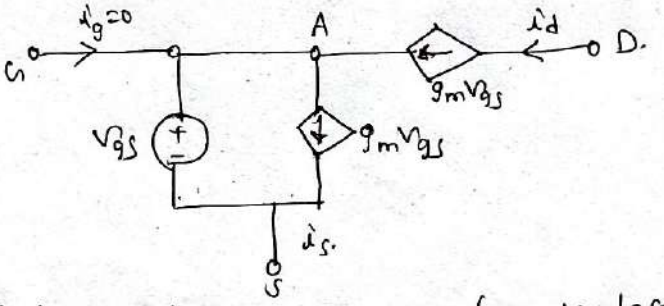
The π-model of MOSFET is given by



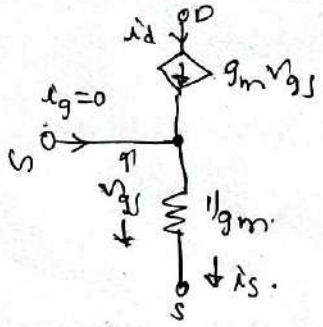
By adding a second $g_m V_{gs}$ current source in series with the original source. so that it does not change the terminal current



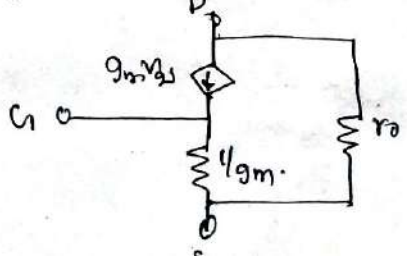
The newly created node 'A' is now joined to the gate terminal G, so that the gate current does not change. and remaing as zero.



Now $g_m V_{gs}$ is connected across V_{gs}. we can replace this sources with a resistance with a value of $\frac{V_{gs}}{g_m V_{gs}} = \frac{1}{g_m}$.

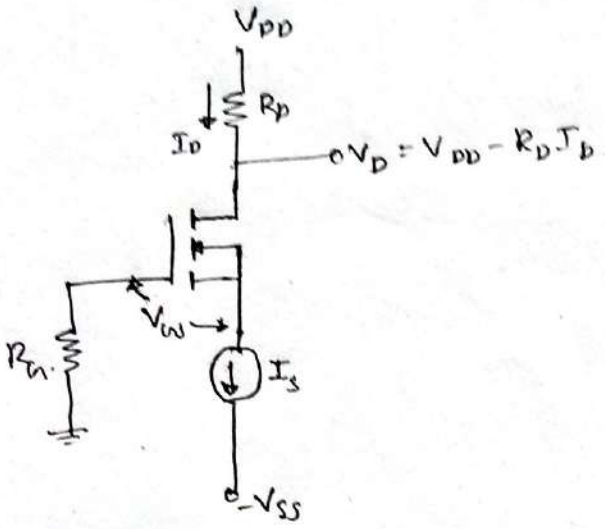


Here the resistance between gate and source. looking into the source is $1/g_m$. The resistance between gate and source looking into the gate is infinite. By considering the output resistance, the T-model is.



Single stage MOS Amplifiers

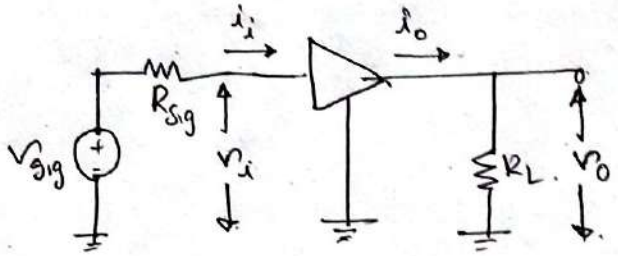
In discrete circuits the MOSFET source is usually tied to the substrate, then body effect is not considered. The basic structure of the circuit used to realize single stage discrete MOS Amplifier circuit is given as.



Characterizing Amplifiers

In MOSFET, there is an internal feedback between the input resistance and load resistance and also between the output resistance and resistance of signal source. So it is called as nonunilateral amplifiers

The general circuit of any amplifier is.



The input resistance with no load $R_i = \frac{v_i}{i_i} \Big|_{R_L=\infty}$

The input resistance $R_{in} = \frac{v_i}{i_i}$

The open circuit voltage gain $A_{vo} = \frac{v_o}{v_i} \Big|_{R_L=\infty}$

The voltage gain $A_v = \frac{v_o}{v_i}$

The short circuit current gain $A_{is} = \frac{i_o}{i_i} \Big|_{R_L=0}$

The current gain $A_i = \frac{i_o}{i_i}$

Short circuit conductance $= g_m = \frac{i_o}{v_i} \Big|_{R_L=0}$

Output resistance of Amplifier $R_o = \frac{v_o}{i_o} \Big|_{v_i = 0}$

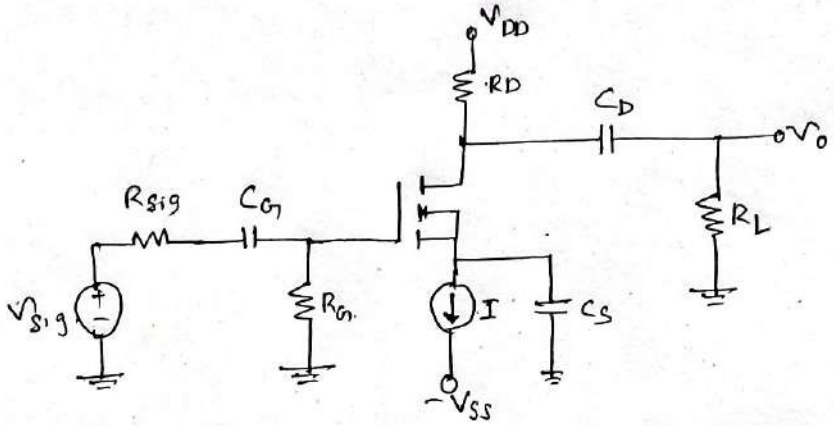
output resistance $R_{out} = \frac{v_o}{i_o} \Big|_{v_{sig}=0}$

open circuit overall voltage gain $G_{vo} = \frac{v_o}{v_{sig}} \Big|_{R_L = \infty}$

Overall voltage gain $= G_v = \frac{v_o}{v_{sig}}$.

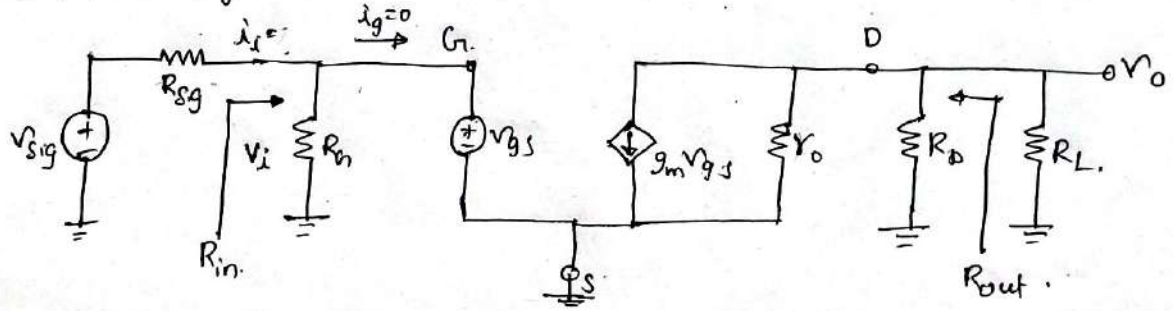
Common Source Amplifier

The common source Amplifier circuit is given by



* To establish a signal ground at source, a large capacitor C_S is connected between source and ground. It is called as bypass capacitor.
* C_G and C_D are coupling capacitors connected at Gate and drain terminals. The voltage signal at drain is coupled to the Load resistance R_L through C_D.

The small signal model of CS Amplifier is.



The terminal characteristics of CS Amplifier are input resistance, voltage gain and output resistance.

Here $R_{in} = R_i$

$R_{out} = R_o$

At input $i_g = 0$

$R_{in} = R_G$.

$$V_i = V_{sig}\frac{R_{in}}{R_{in}+R_{sig}} = V_{sig}\frac{R_G}{R_G+R_{sig}}$$

Generally R_G is selected as very high value.

$$R_G >> R_{sig} \Rightarrow R_G + R_{sig} \simeq R_G.$$

$$V_i = V_{sig}.$$

Now $V_{gs} = V_i$

$$V_o = -g_m V_{gs}(r_o \| R_D \| R_L)$$

$$\frac{V_o}{V_{gs}} = A_v = -g_m(r_o \| R_D \| R_L)$$

Open circuit voltage gain $A_{vo} = -g_m(r_o \| R_D)$

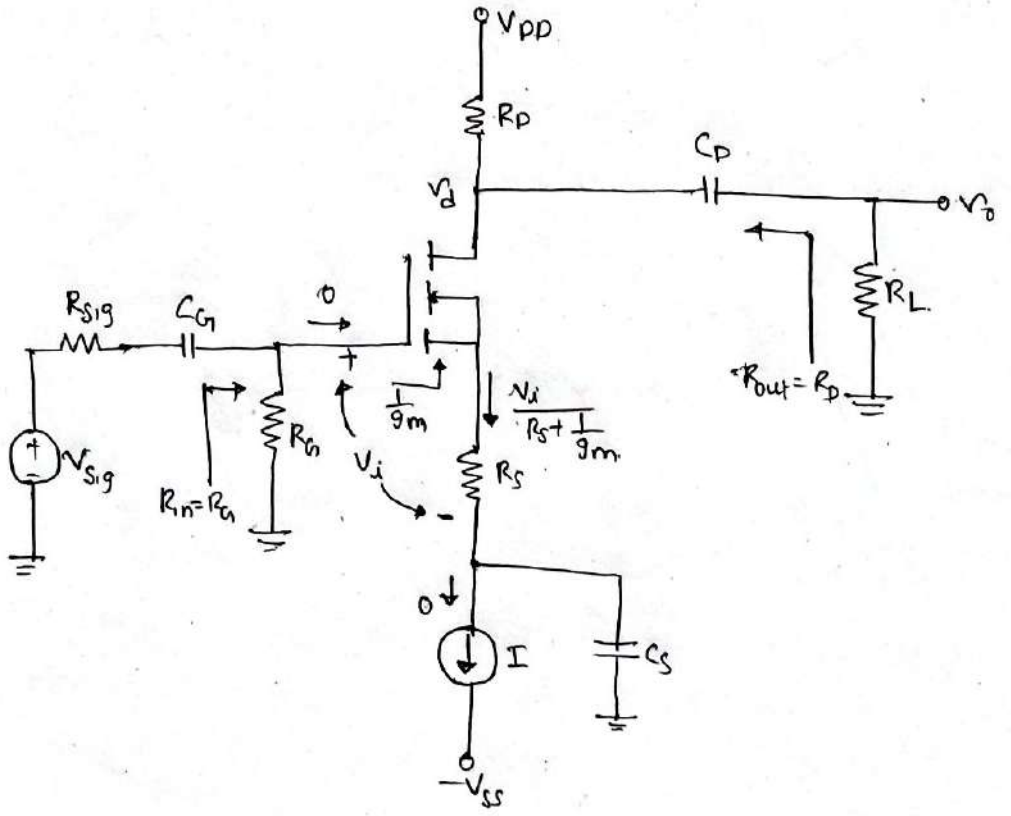
Overall voltage gain $G_v = \frac{R_{in}}{R_{in}+R_{sig}} A_v$

$$= -\frac{R_G}{R_G+R_{sig}} g_m(r_o \| R_D \| R_L)$$

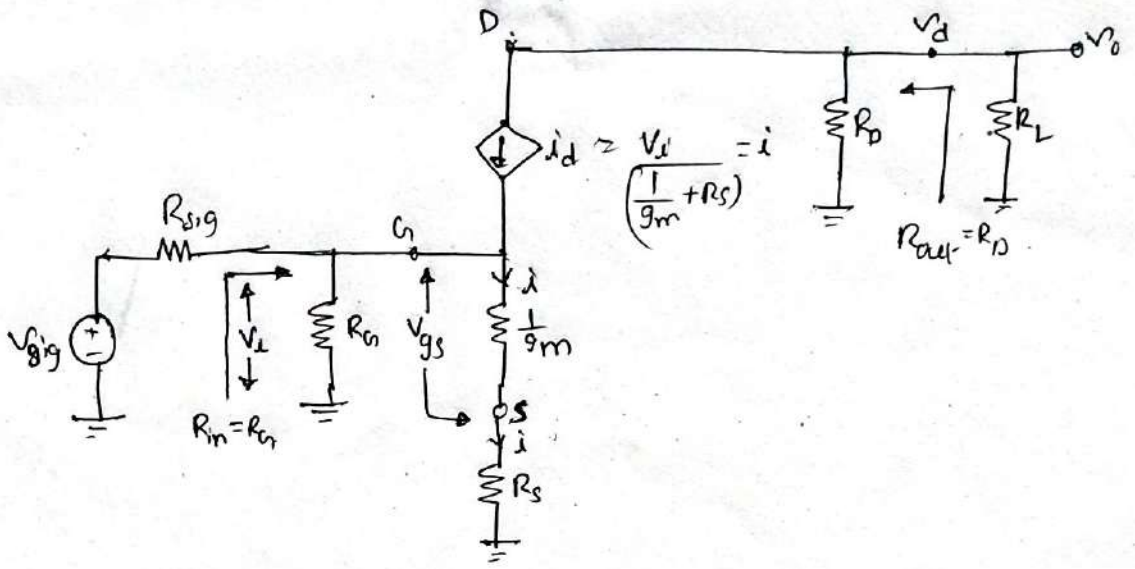
Output resistance $R_{out} = r_o \| R_D$

Common source Amplifier with Source Resistance.

The common source amplifier with a resistance R_S in the source lead is given by.



the small signal equivalent circuit with r_o is neglected is given as



Here $R_{in} = R_i = R_G$.

$$v_i = \frac{R_G}{R_G + R_{sig}} \cdot v_{sig}$$

$$v_{gs} = v_i \cdot \frac{(\frac{1}{g_m})}{\frac{1}{g_m} + R_S} = \frac{v_i}{1 + g_m R_S}$$

Here R_S is to control the magnitude of v_{gs}, ensure that v_{gs} does not become too large and cause unacceptably high nonlinear distortion.

$$i_d = i = \frac{v_i}{\frac{1}{g_m} + R_S} = \frac{g_m v_i}{1 + g_m R_S}$$

$$v_o = -i_d (R_D \| R_L)$$

$$= \frac{-g_m v_i}{(1 + g_m R_S)} \cdot (R_D \| R_L)$$

$$A_v = \frac{v_o}{v_i} = \frac{-g_m (R_D \| R_L)}{1 + g_m R_S}$$

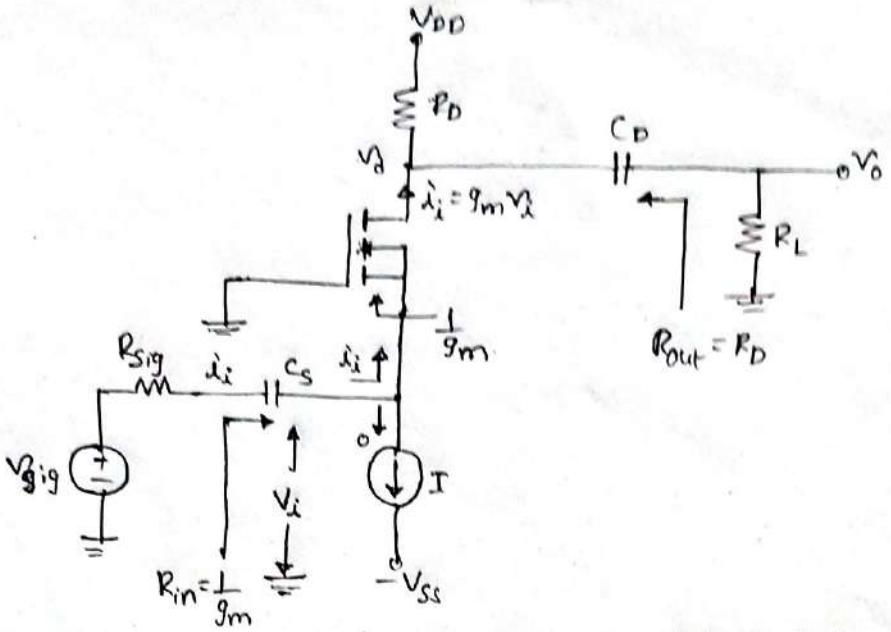
if $R_L = \infty$, then $A_{vo} = \frac{-g_m R_D}{1 + g_m R_S}$

overall voltage gain $G_v = -\frac{R_G}{R_G + R_{sig}} \cdot \frac{g_m (R_D \| R_L)}{1 + g_m R_S}$

The action of R_S that reduces the variability of I_D in a small variation. Because of this action in reducing the gain, R_S is called as source degeneration resistance.

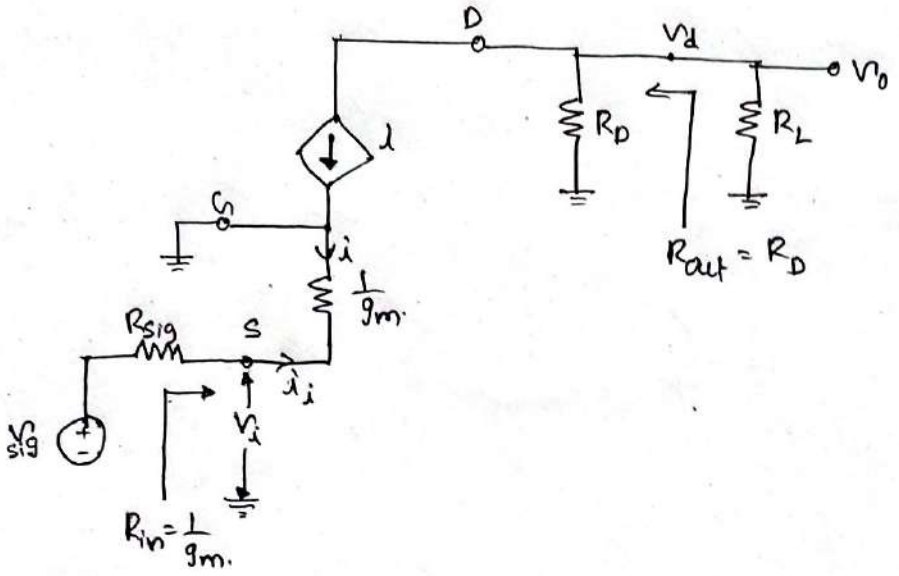
Common Gate Amplifier

The Common Gate Amplifier circuit is given as.



* It is also called as grounded Gate Amplifier because a signal ground is established at gate terminal.
* The input signal is applied to the source and output is taken at the drain.
* Both the DC and AC voltages at the gate are to be zero, the gate is directly connected to ground. C_S & C_D are coupling capacitors.

The small signal equivalent circuit of the CG Amplifier is given as



From the circuit $R_{in} = \frac{1}{g_m}$

$$V_i = V_{sig} \cdot \frac{R_{in}}{R_{in} + R_{sig}} = V_{sig} \cdot \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_{sig}}$$

$$V_i = V_{sig} \frac{1}{1 + g_m R_{sig}}$$

Here $R_{sig} << \frac{1}{g_m}$

The current $i_i = \frac{V_i}{R_{in}} = \frac{V_i}{\left(\frac{1}{g_m}\right)} = g_m V_i$

The drain current $i_d = i = -i_i = -g_m V_i$

$$V_o = V_d = -i_d (R_D \| R_L)$$
$$= g_m V_i (R_D \| R_L)$$

Voltage gain $A_v = g_m (R_D \| R_L)$

Open circuit voltage gain $A_{vo} = g_m R_D$

overall voltage gain $G_v = \frac{R_{in}}{R_{in} + R_{sig}} . A_v$

$$= \frac{\frac{1}{g_m}}{\frac{1}{g_m} + R_{sig}} . A_v = \frac{A_v}{1 + g_m R_{sig}}$$

$$G_v = \frac{g_m (R_D \| R_L)}{1 + g_m R_{sig}}$$

output resistance $R_{out} = R_o = R_D$

This CG Amplifier has very low input resistance.

If the CG Amplifier is fed with a signal current source i_{sig} having an internal resistance R_{sig}.

$$\text{So } R_{in} = \frac{1}{g_m}$$

$$i_i = i_{sig} \frac{R_{sig}}{R_{sig} + R_{in}}$$

$$= i_{sig} \frac{R_{sig}}{R_{sig} + \frac{1}{g_m}}$$

$$R_{sig} >> \frac{1}{g_m}$$

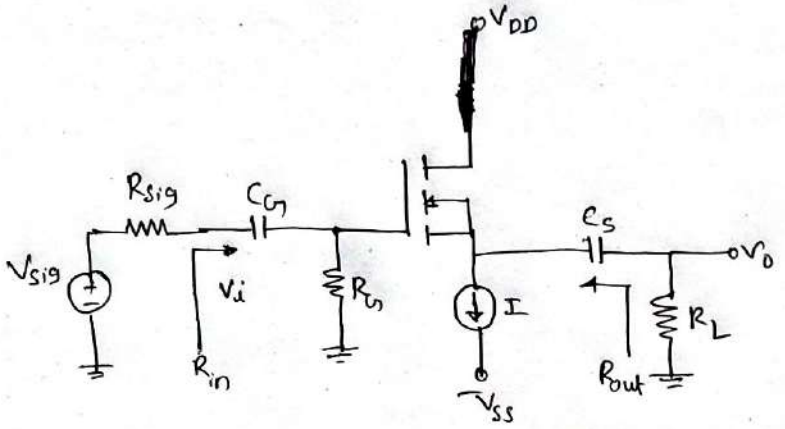
$$i_i = i_{sig}$$

The MOSFET reproduces this current in the drain terminal at a much higher output resistance.

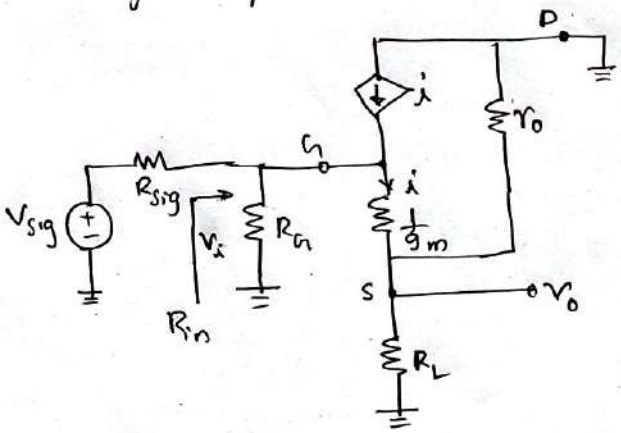
This circuit is called as unity gain current amplifier or current follower.

Common Drain Amplifier

It is also called as grounded drain amplifier or source follower. Here input is applied to Gate and output is taken from source. The Common drain Amplifier is given as



* Since the drain is to function as a signal ground, there is no need of R_D. The input signal is coupled to C_G and output signal is coupled through C_S to a load resistance R_L.
* The small signal equivalent circuit is given as



$$R_{in} = R_G$$

$$v_i = V_{sig}\frac{R_{in}}{R_{in}+R_{sig}} = V_{sig}\cdot\frac{R_h}{R_h+R_{sig}}$$

$$R_h >>> R_{sig}$$

$$V_i = V_{sig}$$

$$V_0 = v_i \cdot \frac{R_L \| r_o}{\left(R_L \| r_o + \frac{1}{g_m}\right)}$$

$$A_r = \frac{(R_L \| r_o)}{(R_L \| r_o) + \frac{1}{g_m}}$$

Open Circuit voltage gain $A_{ro} = \dfrac{r_o}{r_o + \frac{1}{g_m}}$, $r_o >> R_L$.

But $r_o >> \frac{1}{g_m}$.

$A_{vo} \simeq 1$ → so it is called as source follower.

Over all voltage gain $G_v = \frac{R_G}{R_G + R_{sig}} \cdot \frac{R_L \| r_o}{R_L \| r_o + \frac{1}{g_m}}$.

$G_v = \frac{R_G}{R_G + R_{sig}} \cdot \frac{r_o}{r_o + \frac{1}{g_m}}$.

if $R_G >> R_{sig}$
$r_o >> \frac{1}{g_m}$
$r_o >> R_L$

$G_v \simeq 1$

Output resistance $R_{out} = \frac{1}{g_m} \| r_o$.

if $r_o >> \frac{1}{g_m}$

then $R_{out} = \frac{1}{g_m}$.

Parameter	CS Amplifier	CS Amplifier with R_s	CG Amplifier	CD Amplifier.
R_{in}	R_G.	R_G	$\frac{1}{g_m}$	R_G.
A_v	$-g_m(r_o \| R_D \| R_L)$	$\frac{-g_m(R_D \| R_L)}{1 + g_m R_s}$.	$g_m(R_D \| R_L)$	$\frac{r_o \| R_L}{(r_o \| R_L) + \frac{1}{g_m}}$.
G_v	$\frac{R_G}{R_G + R_{sig}} g_m(r_o \| R_D \| R_L)$	$\frac{R_G}{R_G + R_{sig}} \frac{g_m(R_D \| R_L)}{1 + g_m R_s}$	$\frac{g_m(R_D \| R_L)}{1 + g_m R_{sig}}$	$\frac{R_G}{R_G + R_{sig}} \frac{r_o \| R_L}{(r_o \| R_L + \frac{1}{g_m})}$
R_{out}	$r_o \| R_D$	R_D	R_D	$r_o \| \frac{1}{g_m}$.