VISVESVARAYA TECHNOLOGICAL UNIVERSITY

JNANA SANGAMA, BELGAVI -590 014

Study Materials

Electronics Principals Circuites (BEC303)

(IPCC)

(Effective from the academic Year 2025-2026)

SEMESTER – III

Subject Code: BEC303

(Choice Based Credit System)

Prepared by:	HOD
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Department Of Information Science and Engineering

Akshaya Institute of Technology

(Affiliated to VTU, Belgum& Approved by AICTE, New Delhi)

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Akshaya Institute of Technology

(Recognized by AICTE, New Delhi and Affiliated to Visvesvaraya Technological , University, Belagavi)
Akshaya Institute of Technology lingapura, Obalapura post, Koratagere Road, Tumakuru-distric-572106, Karnataka State, INDIA.

Year: 2025 - 2026

Electronics Principals Circuites (BEC303)

(IPCCBEC303)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

(Effective from the academic Year 2025-26)
SEMESTER – III
Subject Code: BEC303
(Choice Based Credit System)

STUDENT'S NAME: ……

USN: ……

BRANCH: ……

SECTION: …… **YEAR:** ……

Vision

To produce competent engineering professionals in the field of Electronics & Communincations Engineering by imparting value based quality technical education to meetthe societal needs and develop socially responsible citizens

Mission

M1: To provide strong fundamentals and technical skills in the field of Electronics and communication Engineering through effective teaching learning process.

M2: Enhancing employ ability of the students by providing skills in the fields of VLSI, Embedded systems

M3: Encourage the students to participate in co curricular and extra curricular activities that creates a spirit of social responsibility and leadership qualities.

Program Outcomes

Sl. No.	Description	POs
1	**Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and computer science and business systems to the solution of complex engineering and societal problems.	PO1
2	**Problem analysis:** Identify, formulate, review research literature, and analyze complex engineering and business problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.	PO2
3	**Design/development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.	PO3
4	**Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.	PO4
5	**Modern tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations	PO5
6	**The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering and business practices.	PO6
7	**Environment and sustainability:** Understand the impact of the professional engineering solutions in business societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.	PO7
8	**Ethics:** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering and business practices.	PO8
9	**Individual and team work:** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.	PO9
10	**Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.	PO10
11	**Project management and finance:** Demonstrate knowledge and understanding of the engineering, business and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.	PO11
12	**Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.	PO12

Electronic Principles and Circuits		Semester	3
Course Code	**BEC303**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	3:0:2	SEE Marks	50
Total Hours of Pedagogy	40 hours Theory + 8-10 Lab slots	Total Marks	100
Credits	04	Exam Hours	3
Examination nature (SEE)	Theory/Practical		

Course objectives:

This course will enable students to

- Design and analyse the BJT circuits as an amplifier and voltage regulation.
- Design of MOSFET Amplifiers and analyse the basic amplifier configurations using small signal equivalent circuit models
- Design of operational amplifiers circuits as Comparators, DAC and filters.
- Understand the concept of positive and negative feedback.
- Analyze Power amplifier circuits in different modes of operation.
- Construct Feedback and Oscillator circuits using FET.
- Understand the thyristor operation and the different types of thyristors.

Teaching-Learning Process (General Instructions)

These are sample Strategies, which teacher can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain evolution of communication technologies.
3. Encourage collaborative (Group) Learning in the class
4.Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyze information rather than simply recall it.
6. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
7. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.

MODULE-1

BJT AC models: Base Biased Amplifier, Emitter Biased Amplifier, Small Signal Operation, AC Beta, AC Resistance of the emitter diode, Two transistor models, Analyzing an amplifier.

Voltage Amplifiers: Voltage gain, Multistage Amplifiers.

CC and CB Amplifiers: CC Amplifier, Output Impedance, Cascading CE and CC, Darlington Connections, Voltage regulation, The Common base Amplifier.

[Text1]

MODULE-2

MOSFET

Biasing in MOS amplifier circuits: Fixing VGS, Fixing VG, Drain to Gate feedback resistor.

Small signal operation and modelling: The DC bias point, signal current in drain, voltage gain, small signal equivalent circuit models, transconductance, The T equivalent circuit model.

MOSFET Amplifier configuration: Basic configurations, characterizing amplifiers, CS amplifier with and without source resistance, The Common Gate Amplifier, Source follower.

MODULE-3

Linear Opamp Circuits: Summing Amplifier and D/A Converter, Nonlinear Op-amp Circuits: Comparator with zero reference, Comparator with non-zero references. Comparator with Hysteresis.

Oscillator: Theory of Sinusoidal Oscillation, The Wein-Bridge Oscillator, RC Phase Shift Oscillator, The Colpitts Oscillator, Hartley Oscillator, Crystal Oscillator.

The 555 timer: Monostable Operation, Astable Operation.

[Text1]

MODULE-4

Negative Feedback: Four Types of Negative Feedback, VCVS Voltage gain, Other VCVS Equations, ICVS Amplifier, VCIS Amplifier, ICIS Amplifier (No Mathematical Derivation).

Active Filters: Ideal Responses, First Order Stages, VCVS Unity Gain Second Order Low pass Filters, VCVS Equal Component Low Pass Filters, VCVS High Pass Filters, MFB Bandpass Filters, Bandstop Filters.

[Text1]

MODULE-5

Power Amplifiers: Amplifier terms, Two load lines, Class A Operation, Class B operation, Class B push pull emitter follower, Class C Operation.

Thyristors: The four layer Diode, SCR, SCR Phase control, Bidirectional Thyristors, IGBTs, Other Thyristors.

[Text1]

PRACTICAL COMPONENT OF IPCC *(Experiments can be conducted either using any circuit simulation software or discrete components)*

Sl.NO	Experiments
1	Design and Test (i) Bridge Rectifier with Capacitor Input Filter (ii) Zener voltage regulator
2	Design and Test Biased Clippers – a)Positive, b) Negative , c) Positive-Negative Positive and Negative Clampers with and without Reference.
3	Plot the transfer and drain characteristics of a JFET and calculate its drain resistance, mutual conductance and amplification factor.
4	Plot the transfer and drain characteristics of n-channel MOSFET and calculate its parameters, namely; drain resistance, mutual conductance and amplification factor.
5	Design and test (i) Emitter Follower , (ii) Darlington Connection
6	Design and plot the frequency response of Common Source JFET/MOSFET amplifier
7	Test the Opamp Comparator with zero and non zero reference and obtain the Hysteresis curve.
8	Design and test Full wave Controlled rectifier using RC triggering circuit.
9	Design and test Precision Half wave and full wave rectifiers using Opamp
10	Design and test RC phase shift oscillator

Course outcomes (Course Skill Set):

At the end of the course, the student will be able to:

1. Understand the characteristics of BJTs and FETs for switching and amplifier circuits.
2. Design and analyze amplifiers and oscillators with different circuit configurations and biasing conditions.
3. Understand the feedback topologies and approximations in the design of amplifiers and oscillators.
4. Design of circuits using linear ICs for wide range applications such as ADC, DAC, filters and timers.
5. Understand the power electronic device components and its functions for basic power electronic circuits.

Assessment Details (both CIE and SEE)

The weightage of Continuous Internal Evaluation (CIE) is 50% and for Semester End Exam (SEE) is 50%. The minimum passing mark for the CIE is 40% of the maximum marks (20 marks out of 50) and for the SEE minimum passing mark is 35% of the maximum marks (18 out of 50 marks). The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

The IPCC means the practical portion integrated with the theory of the course. CIE marks for the theory component are **25 marks** and that for the practical component is **25 marks**.

CIE for the theory component of the IPCC

- 25 marks for the theory component are split into **15 marks** for two Internal Assessment Tests (Two Tests, each of 15 Marks with 01-hour duration, are to be conducted) and **10 marks** for other assessment methods mentioned in 22OB4.2. The first test at the end of 40-50% coverage of the syllabus and the second test after covering 85-90% of the syllabus.

- Scaled-down marks of the sum of two tests and other assessment methods will be CIE marks for the theory component of IPCC (that is for **25 marks)**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the theory component of IPCC.

CIE for the practical component of the IPCC

- **15 marks** for the conduction of the experiment and preparation of laboratory record, and **10 marks** for the test to be conducted after the completion of all the laboratory sessions.
- On completion of every experiment/program in the laboratory, the students shall be evaluated including viva-voce and marks shall be awarded on the same day.
- The CIE marks awarded in the case of the Practical component shall be based on the continuous evaluation of the laboratory report. Each experiment report can be evaluated for 10 marks. Marks of all experiments' write-ups are added and scaled down to **15 marks**.
- The laboratory test **(duration 02/03 hours)** after completion of all the experiments shall be conducted for 50 marks and scaled down to **10 marks.**
- Scaled-down marks of write-up evaluations and tests added will be CIE marks for the laboratory component of IPCC for **25 marks**.
- The student has to secure 40% of 25 marks to qualify in the CIE of the practical component of the IPCC.

SEE for IPCC

Theory SEE will be conducted by University as per the scheduled timetable, with common question papers for the course (**duration 03 hours**)

1. The question paper will have ten questions. Each question is set for 20 marks.
2. There will be 2 questions from each module. Each of the two questions under a module (with a maximum of 3 sub-questions), **should have a mix of topics** under that module.
3. The students have to answer 5 full questions, selecting one full question from each module.
4. Marks scored by the student shall be proportionally scaled down to 50 Marks

The theory portion of the IPCC shall be for both CIE and SEE, whereas the practical portion will have a CIE component only. Questions mentioned in the SEE paper may include questions from the practical component.

- The minimum marks to be secured in CIE to appear for SEE shall be 10 (40% of maximum marks-25) in the theory component and 10 (40% of maximum marks -25) in the practical component. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included**.** The maximum of 04/05 sub-questions are to be set from the practical component of IPCC, the total marks of all questions should not be more than 20 marks.
- SEE will be conducted for 100 marks and students shall secure 35% of the maximum marks to qualify for the SEE. Marks secured will be scaled down to 50.
- The student is declared as a pass in the course if he/she secures a minimum of 40% (40 marks out of 100) in the sum total of the CIE (Continuous Internal Evaluation) and SEE (Semester End Examination) taken together.

Suggested Learning Resources:

Books

1. Albert Malvino, David J Bates, Electronic Principles, 7th Edition, Mc Graw Hill Education, 2017, ISBN:978-0-07-063424-4.
2. Microelectronic Circuits, Theory and Applications, Adel S Sedra, Kenneth C Smith, 6thEdition, Oxford, 2015.ISBN:978-0-19-808913-1

Web links and Video Lectures (e-Resources):

1. Integrated Electronics: Analog and Digital Circuits and Systems, Jacob Millman, Christos C. Halkias, McGraw-Hill, 2015.
2. Electronic Devices and Circuit, Boylestad & Nashelsky, Eleventh Edition, Pearson, January 2015.

Activity Based Learning (Suggested Activities in Class)/ Practical Based learning

Electronic Principles and Circuits

Module - I

Transistor Biasing

→ We can operate transistor in three regions cut-off region, Saturation region and Active region.

* Transistor is operated in cut-off region by keeping the Emitter-Base junction in Reverse Bias mode and collector Base Junction in Reverse Bias mode.
* Transistor is operated in saturation region by keeping the Emitter-Base Junction in Forward Bias mode and Collector Base junction in forward Bias mode.
* Transistor is operated in Active region by keeping the Emitter Base junction in Forward Bias mode and Collector Base junction in Reverse Bias mode.

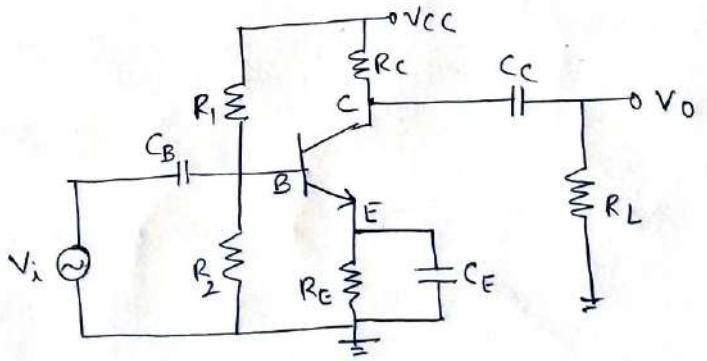
→ In order to operate the transistor in the desired region we have to apply external DC voltage to the two junctions of the transistor. This is called as biasing of the transistor.

→ When we bias a transistor we establish a certain current and voltage conditions for the transistor. These conditions are known as operating conditions or quiescent conditions.

The DC load line and Operating point

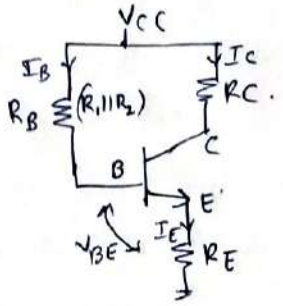
For this Analysis, we are considing common Emitter configuration of a transistor.

Let us consider common Emitter Amplifier circuit



* The transistor is biased with supply voltage V_{cc} such that the base emitter junction is forward biased and the collector Base junction is reverse biased.

* In the absence of AC signal, the capacitors act as open circuit, so the equivalent circuit is given as:



Applying Kirchoff's voltage law to the collector circuit

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

but $I_C \simeq I_E$

$$V_{CC} - I_C (R_C + R_E) - V_{CE} = 0$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

Applying Kirchoff's voltage law to the Base circuit.

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

but $I_E = (1+\beta) I_B$.

$$V_{CC} - I_B R_B - V_{BE} - (1+\beta) I_B R_E = 0$$

$$I_B \left[R_B + (1+\beta) R_E \right] = V_{CC} - V_{BE}$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}}$$

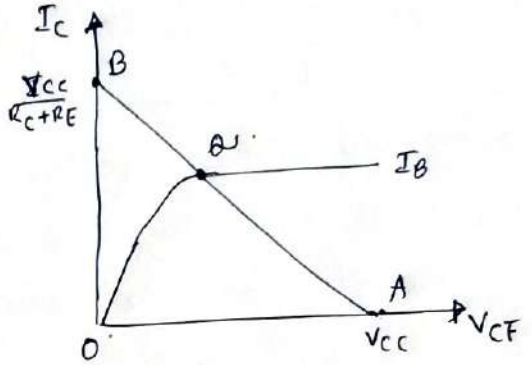
So $\boxed{I_C = \beta I_B}$

* In the output voltage equation, we make two conditions.

a) $I_C = 0 \Rightarrow V_{CE} = V_{CC}. \Rightarrow$ X-axis point - A

b) $V_{CE} = 0 \Rightarrow I_C = \frac{V_{CC}}{R_C + R_E} \Rightarrow$ Y-axis point - B

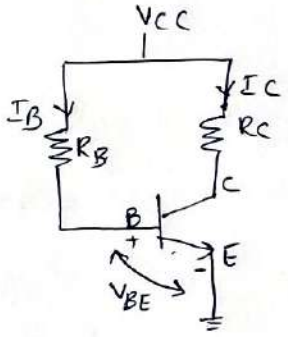
Now we are plotting the output characteristics of a transistor with I_C on y-axis and V_{CE} on x-axis.



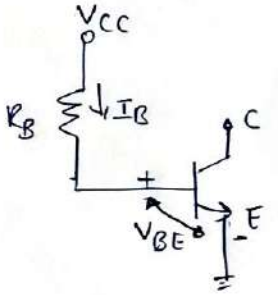
* We are representing the points A and B and a line is drawn between them. This is called DC load line
* The 'DC' word indicates that only dc conditions are considered, the input signal is assumed to be zero.
* If we draw the characteristic curve for some value of I_B, then the intersection of this curve with load line is called operating point.
* This point is a fixed value, so it is called as Quiescent point. The point A is named as V_{CE} (cut-off) and the point B is named as I_C (Saturation)

Base Bias Method

This is also called as Fixed Bias. Here we have only Base resistor connected between supply and Base terminal of transistor. The Circuit is given as.



* Here Base is the input terminal and collector is output terminal By considering the Base circuit.



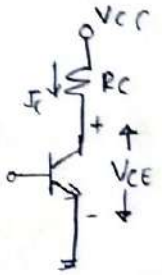
Applying Kirchhoff's voltage law to the above circuit

$$V_{CC} - I_B R_B - V_{BE} = 0.$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

* The supply voltage V_{CC} is a fixed value, R_B is a fixed value V_{BE} is also fixed value. So I_B is fixed value. Hence this circuit is called as fixed bias circuit.

* By considering the collector circuit



Applying Kirchoff's voltage law to the collector circuit we get

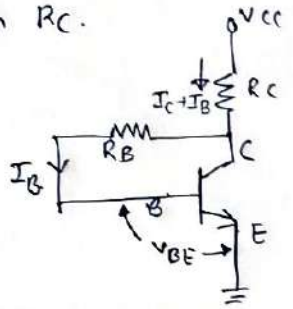
$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$I_C = \beta I_B$$

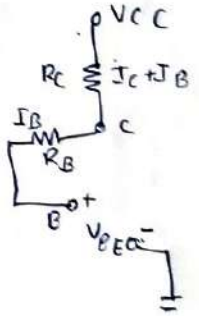
Collector to Base Bias method

* Here the biasing resistor is connected between the collector and the base of the transistor. So I_B flows through R_B and $I_C + I_B$ flows through R_C.



It is also called as collector-feedback Bias.

* Applying KVL to the base circuit.



$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} = 0$$

$$I_C = (\beta) I_B$$

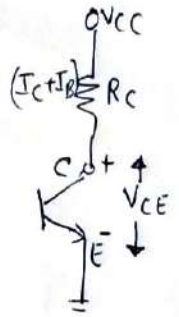
$$V_{CC} - V_{BE} = (\beta + 1) R_C I_B + I_B R_B$$

$$I_B \left[R_B + (\beta + 1) R_C \right] = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_C}$$

$$I_C = \beta I_B.$$

* Applying KVL to collector circuit



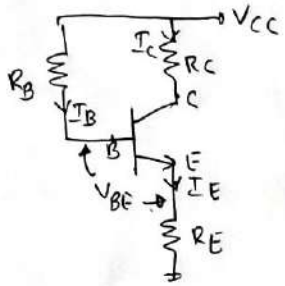
$$V_{CC} - (I_C + I_B) R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - \left(I_C + \frac{I_C}{\beta}\right) R_C$$

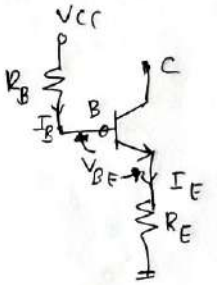
$$\boxed{V_{CE} = V_{CC} - \frac{(\beta+1)}{\beta} I_C R_C}$$

Emitter Bias Method

* An emitter resistor is added to the emitter terminal of the fixed bias circuit



* Applying KVL to Base Circuit, we get



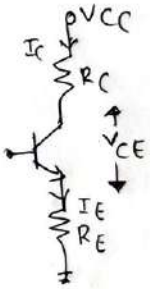
$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_E = (\beta+1) I_B$$

$$V_{CC} - V_{BE} = I_B R_B + (\beta+1) I_B \cdot R_E$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1) R_E}} \rightarrow I_C = \beta I_B$$

* Applying KVL to collector circuit, we get



$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

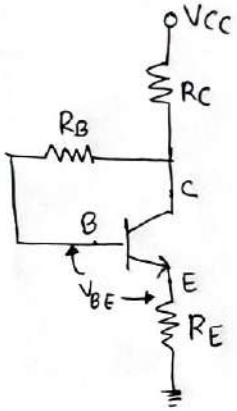
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \simeq I_C$$

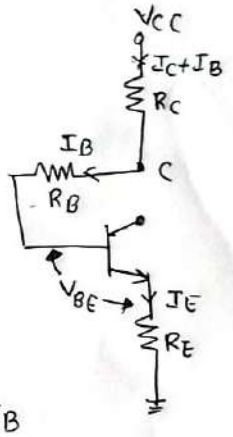
$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

Collector and Emitter Feedback Bias

This circuit contains resistor at each terminal and the circuit is given by



* By applying KVL to Base circuit, we get:



$$V_{CC} - (I_C + I_B) R_C - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_e = \beta I_B$$

$$I_e = (\beta+1) I_B$$

$$V_{CC} - V_{BE} = (\beta I_B + I_B) R_C + I_B R_B + (\beta+1) I_B R_E$$

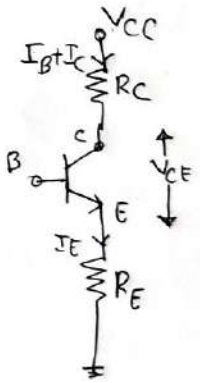
$$= \beta R_C I_B + R_C I_B + (\beta+1) R_E I_B + R_B I_B$$

$$= I_B \left[R_B + (\beta+1) R_C + (\beta+1) R_E \right]$$

$$= I_B \left[R_B + (\beta+1)(R_C + R_E) \right]$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)(R_C + R_E)}} \qquad I_C = \beta I_B$$

* By applying KVL to collector circuit, we get:



$$V_{CC} - (I_C + I_B) R_C - V_{CE} - I_E R_E = 0$$

$$I_C = \beta I_B$$

$$I_B = \frac{I_C}{\beta}$$

$$I_E \simeq I_C$$

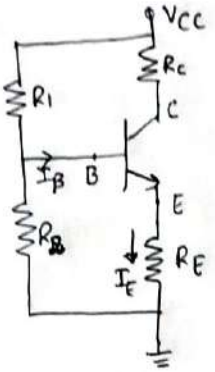
$$V_{CC} - \left(I_C + \frac{I_C}{\beta}\right) R_C - V_{CE} - I_C R_E = 0$$

$$V_{CE} = V_{CC} - \frac{(\beta+1)}{\beta} I_C R_C - I_C R_E$$

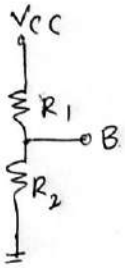
$$\boxed{V_{CE} = V_{CC} - I_C \left[\frac{(\beta+1)}{\beta} R_C + R_E \right]}$$

Voltage Divider Bias

It is also called as Self Bias



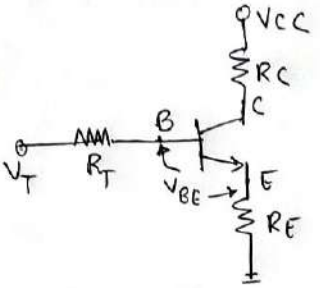
We are applying Thevenin's theorem at the Base terminal



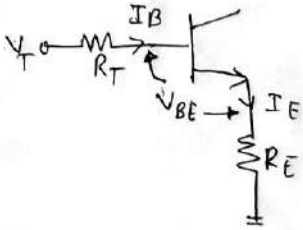
$$V_T = V_{BB} = V_{CC} \cdot \frac{R_2}{R_1 + R_2}$$

$$R_T = R_B = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

So we can redraw the circuit as.



* Applying KVL to the Base terminal, we get



$$V_T - I_B R_T - V_{BE} - I_E R_E = 0$$

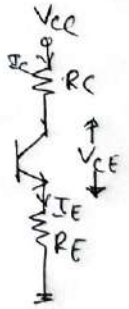
$$I_E = (\beta + 1) I_B$$

$$V_T - V_{BE} = I_B R_T + (\beta + 1) I_B \cdot R_E = 0$$

$$= I_B \left[R_T + (\beta + 1) R_E \right]$$

$$\boxed{I_B = \frac{V_T - V_{BE}}{R_T + (\beta + 1) R_E}} \qquad I_C = \beta I_B$$

* Applying KVL to the collector terminal, we get



$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$I_E \simeq I_C$$

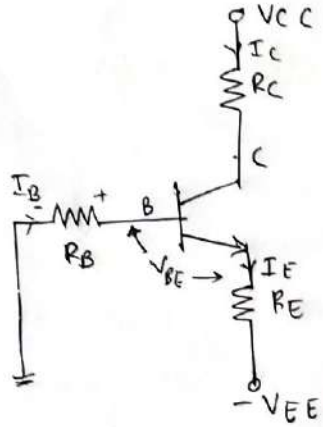
$$V_{CE} = V_{CC} - I_C R_C - I_C R_E$$

$$\boxed{V_{CE} = V_{CC} - I_C (R_C + R_E)}$$

Two Supply Emitter Bias Circuit

→ Here the transistor has two power supplies. The negative supply forward biases the emitter diode. The positive supply reverse biases the collector diode.

→ Since we are connecting negative supply to emitter terminal, this is called as Two supply Emitter Bias.



→ Applying KVL to the base circuit

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$-V_{BE} + V_{EE} = I_B R_B + (\beta+1) I_B R_E$$

$$= I_B \left[R_B + (\beta+1) R_E \right]$$

$$I_B = \frac{|V_{EE}| - V_{BE}}{R_B + (\beta+1) R_E}$$

The absolute value is given to V_{EE}, not to have any confusion regarding the sign and always we consider magnitude.

→ Applying KVL to the collector circuit.

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E - (-V_{EE}) = 0$$

$$V_{CE} = V_{CC} + V_{EE} - I_C R_C - I_E R_E$$

But $I_C \simeq I_E$

$$V_{CE} = V_{CC} + |V_{EE}| - I_C (R_C + R_E)$$

→ DC load line

* To get V_{CE}(cut-off), the I_C value must be zero, so by substituting in V_{CE} equation.

$$V_{CE(cut\text{-}off)} = V_{CC} + |V_{EE}|$$

* To get $I_{C(sat)}$, the V_{CE} value must be zero

$$V_{CE} = V_{CC} + |V_{EE}| - I_C(R_C + R_E)$$

$$0 = V_{CC} + |V_{EE}| - I_{C(sat)}(R_C + R_E)$$

$$I_{C(sat)} = \frac{V_{CC} + |V_{EE}|}{R_C + R_E}$$

Base Biased Amplifier

When we are dealing with amplifiers, capacitors play an important role for AC signals.

→ We call the capacitors as coupling capacitors because the connects the AC signal to the transistor. They only allows AC signal into the amplifier without disturbing Q-point

→ To work properly, the reactance of the capacitor is much lower than the resistance at the lowest frequency of the ac source.

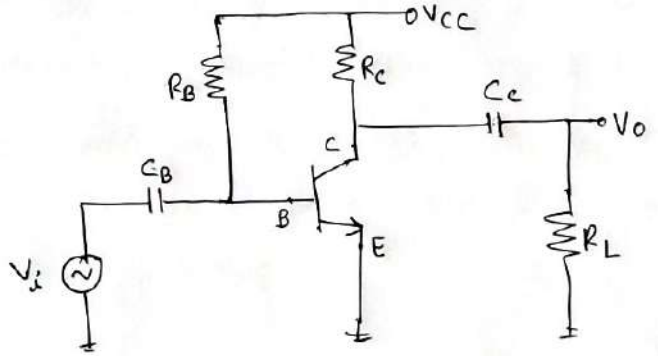
$$\boxed{X_C < 0.1\,R}$$

→ We are using two approximations for the capacitor.

a) For DC analysis, capacitor acts as open circuit

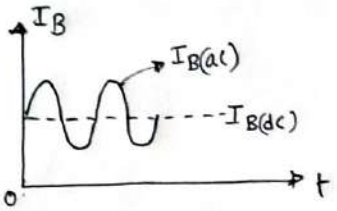
b) For AC analysis, capacitor acts as short circuit

→ The Base Biased Amplifier circuit is given as.

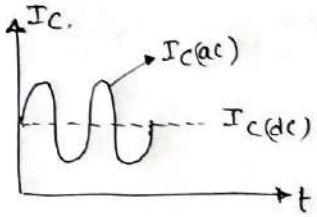


* For a Base Biased circuit, we are connecting AC input signal with Base coupling capacitor and load resistance with collector coupling capacitor.
* We are applying AC input signal to the base which contains AC and DC components. C_B now allows only AC components and blocks DC components.
* So only AC voltage appears between Base and ground. This AC voltage, produces an AC Base current which is added to DC Base current.

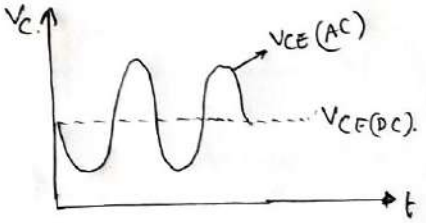
* The total base current will have a DC component and AC component The below waveform shows that an AC component is superimposed on the DC component



* The AC base current produces an amplified value in collector current because of current gain. The collector current has a DC component of $I_{C(dc)}$.

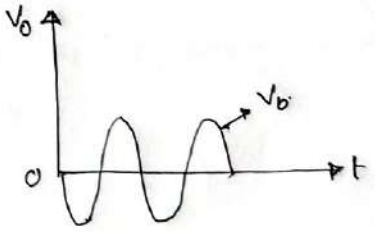


* Since the collector current flows through the collector resistor, it produces a varying voltage across the collector resistor. when this voltage is subtracted from supply voltage, collector voltage is obtained.



* The collector voltage is swinging sinusoidally above and below the DC level $V_{CE(DC)}$. The AC collector voltage is inverted with I/p voltage

* The collector capacitor blocks the $V_{CE(DC)}$ in the output AC signal. and a pure sine wave AC signal is developed across load resistor.



* <u>Voltage gain</u> → It is defined as the AC output voltage divided by the AC input voltage.

$$A_V = \frac{V_{out}}{V_{in}}$$

output voltage $V_{out} = A_V V_{in}$.

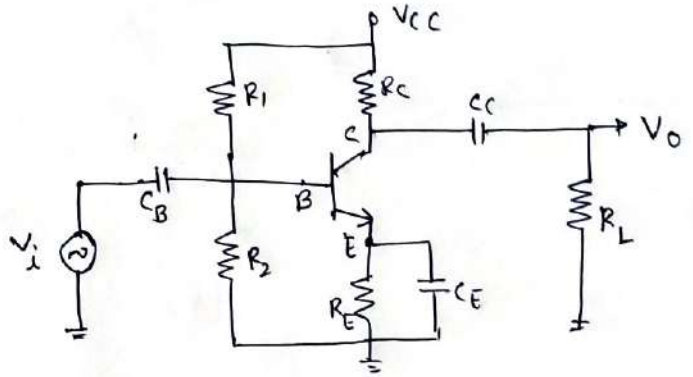
Input voltage $V_{in} = \frac{V_{out}}{A_V}$

Emitter Biased Amplifier

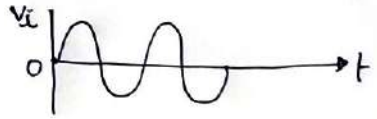
In this amplifier emitter resistor is connected with a bypass capacitor. So we have two types of emitter biased amplifiers
a) VDB amplifier b) TSEB amplifier.

VDB Amplifier

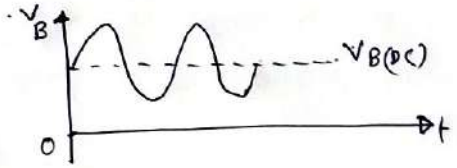
The circuit diagram of VDB amplifier is given as.



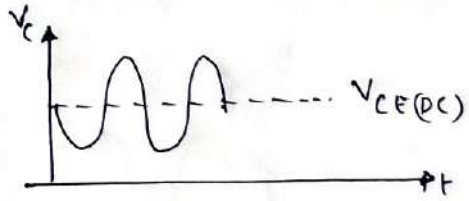
* The Ac input signal is applied to the base of the amplifier This Ac source voltage is a sinusoidal voltage with an average value zero



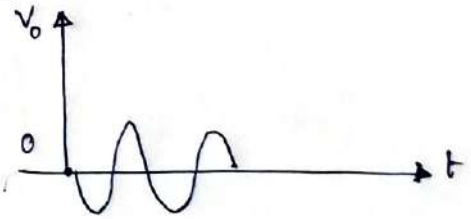
* The base voltage is an Ac voltage superimposed on a DC voltage of $V_{B(dc)}$ and is given as



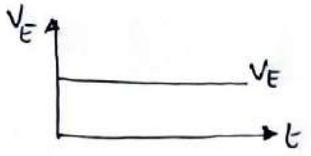
* The collector voltage is an amplified and inverted Ac voltage superimposed on the DC collector voltage of $V_{CE(DC)}$



* Because of presence of collector coupling capacitor, the load voltage is same as collector voltage. but it is pure Ac signal.

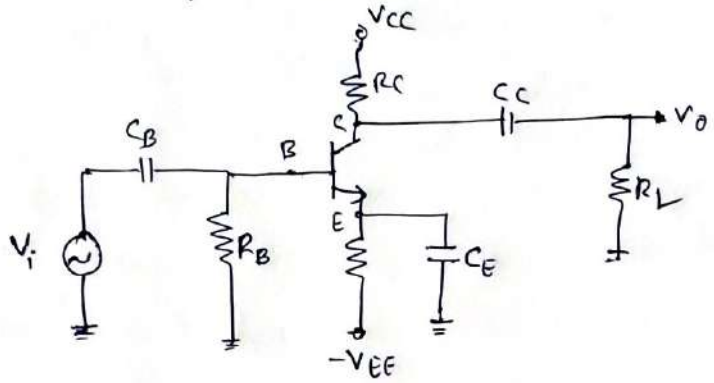


* The voltage at the emitter is a pure DC voltage because it is at AC ground point due to the connection of capacitor.



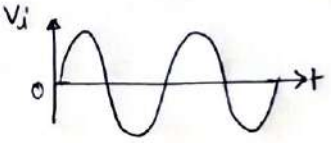
TSEB Amplifier

The circuit diagram of TSEB Amplifier is given as.

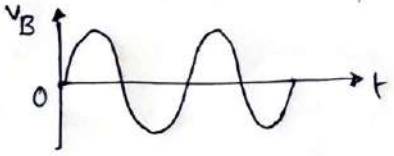


→ The circuit contains two coupling capacitors C_B, C_C and one emitter bypass capacitor

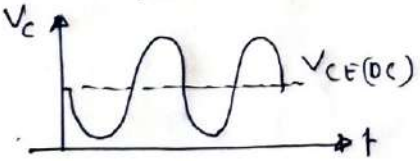
→ The AC source voltage is a small sinusoidal voltage which contains only AC components due to the presence of C_B.



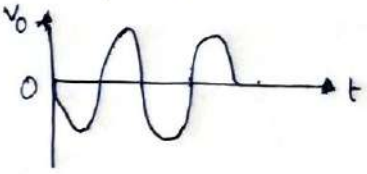
→ The base voltage has a small AC component riding on a small DC component generally considered as zero.



→ The total collector voltage is an inverted sine wave riding on the DC collector voltage $V_{CE(DC)}$.

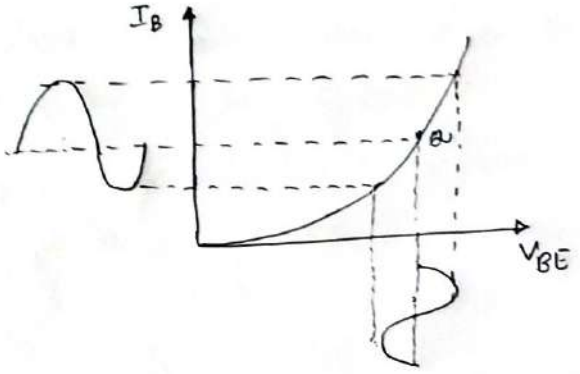


→ The load voltage is same amplified signal with zero DC component due to the presence of C_C.



Small signal operation

A Graph is plotted between the current and voltage for the base emitter diode.



* The base emitter voltage is an AC voltage centered on an DC voltage the AC voltage on the base produces AC base current. This AC base current has a frequency same as AC base voltage.
* The Ac base current has approximately the same shape as the AC base voltage.
* The AC base current is not a perfect replica of the base voltage because of the curvature of the graph.
* Since the graph is curved up, the positive cycle of AC base current is stretched and negative half cycle is compressed. This phenomenon is called <u>distortion</u>
* If we keep Ac base voltage small, we can reduce the distortion. If the signal is small, the graph appears to be linear.
* If the base voltage is small sine wave, the AC base current will be a small sine wave with no stretching or compressing of cycles.
* The total base current consists of a DC component and an AC component. so $I_B = I_{BQ} + i_b$.

$I_B \rightarrow$ total base current, $I_{BQ} \rightarrow$ DC base current

$i_b \rightarrow$ Ac base current.

We can write for emitter current also

$$I_E = I_{EQ} + i_e$$

$I_E \rightarrow$ total emitter current

$I_{EQ} \rightarrow$ DC Emitter current, $i_e \rightarrow$ Ac emitter current.

* To minimize the distortion i_b must be small compared to I_{BQ}.

The small signal operation is

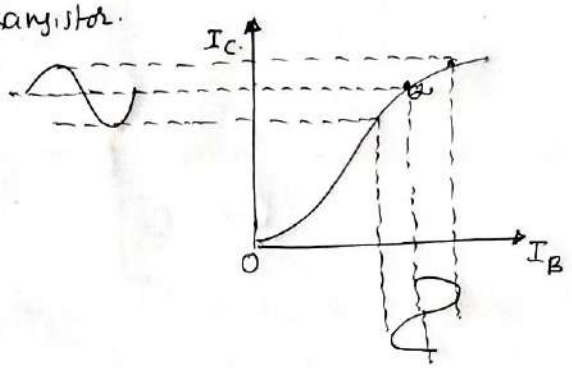
$$i_b < 0.1 I_{BQ} \qquad i_c < 0.1 I_{CQ}$$

* The AC signal is small when AC emitter current is less than the 10 percent of the DC emitter current.

* The amplifiers that satisfy the 10 percent rule is called as Small signal amplifiers. These are used generally at receivers.

AC Beta

A graph is plotted between the input current and output current of a transistor.



* The DC current gain is the ratio of DC Collector current to the DC Base current represented as

$$\beta_{dc} = \frac{I_C}{I_B}.$$

* The AC current gain is the ratio of AC collector current to the AC base current which is represented as.

$$\beta_{ac} = \beta = \frac{i_c}{i_b}.$$

* The AC signal uses only a small part of the graph on both sides of the Q-point. Graphically β is the slope of the curve at Q-point.

* All the DC parameters are represented with capital letters.

I_E, I_C and I_B are DC current

V_E, V_C and V_B are DC voltages.

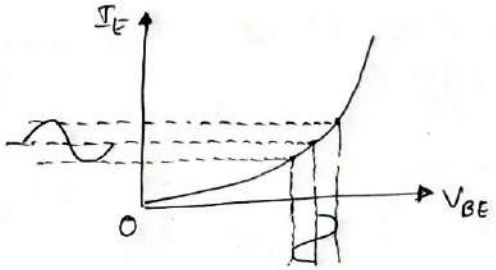
* All the AC parameters are represented with small letters.

i_c, i_e and i_b are AC currents

V_c, V_e and V_b are AC voltages.

AC Resistance of Emitter Diode

A graph is plotted between the voltage and current of emitter diode



* The total emitter current has a DC component and an AC component

$$I_E = I_{E@} + i_e.$$

$I_{E@}$ → DC emitter current
i_e → AC emitter current

* The total base emitter voltage has a DC component and an AC component

$$V_{BE} = V_{BE@} + V_{be}$$

$V_{BE@}$ → DC Base emitter voltage
V_{be} → AC Base emitter voltage

* The AC emitter resistance of the emitter diode is defined as

$$r_e' = \frac{V_{be}}{i_e}$$

The prime(') indicates the resistance is inside the transistor.

* The AC emitter resistance always decreases when the DC emitter current increases because V_{be} is always a constant value.
* The general formula of AC emitter resistance is

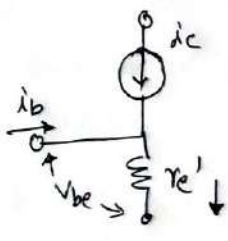
$$r_e' = \frac{25mV}{I_E}$$

Two Transistor Models

To represent the transistor in circuit, it is shown with a circuit called as equivalent circuit. Here we have two models of transistor

T-model

* It is also named as Ebers-Moll model
* The emitter diode of a transistor acts like an AC resistance r_e'
* The collector diode acts like a current source i_c
* Since it looks like a 'T' shape, it is called as T model.



* When an AC input signal drives an amplifier, the AC base emitter voltage V_{be} is developed. It produces an AC base current i_b

* Applying ohm's law at the emitter diode, we have.

$$V_{be} = i_e r_e'$$

* The AC voltage source experiences an input impedance.

$$Z_{in} = \frac{V_{be}}{i_b}$$

$$= \frac{i_e r_e'}{i_b}$$

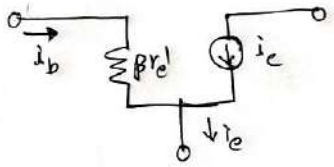
$$i_e \simeq i_c$$

$$Z_{in} = \frac{i_c}{i_b} r_e'$$

$$\boxed{Z_{in} = \beta r_e'}$$

π-Model

It is represented with input impedance of a transistor as $\beta r_e'$. The equivalent circuit model is given as.



Analyzing an Amplifier

To analyze amplifiers, we have to calculate the effect of DC sources and effect of AC sources. We have two types of analysis.

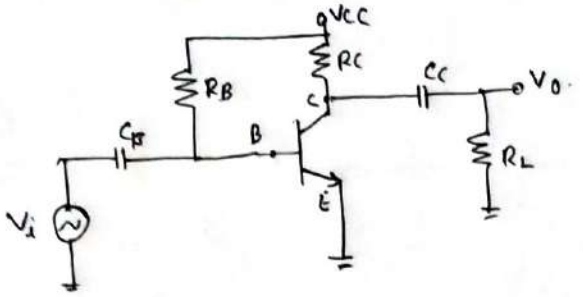
* In DC analysis we will calculate DC voltages and currents. For this, we have to open all the capacitors. Then this circuit is called as DC equivalent circuit.

* In AC analysis, we keep all capacitors in short position and all the DC sources are made to ground. The transistor is to be replaced by T model or π model.

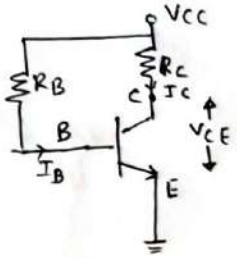
* If circuit is designed by using above techniques it is known as AC equivalent circuit. We will calculate voltage gain, current gain, input impedance and output impedance.

* Base - Biased Amplifier

The general amplifier is given as.

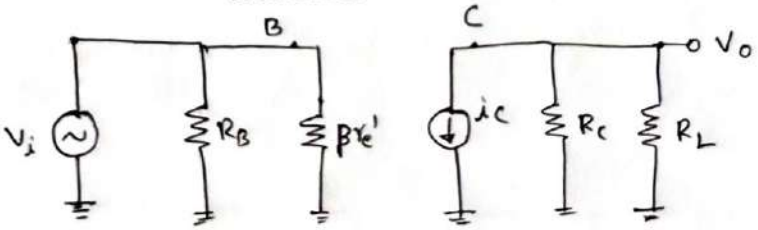


The DC equivalent circuit is designed by removing the capacitors from the circuit using this circuit we can calculate I_B, I_c and V_{CE}, finally we will fix operating point

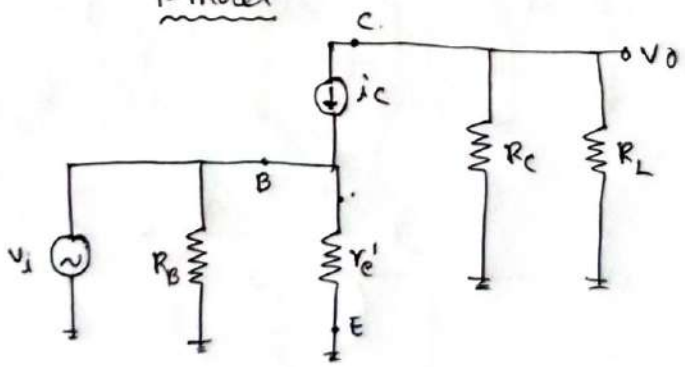


The AC equivalent circuit is designed by short circuiting the capacitors and making voltage sources to ground and by replacing transistor with Π and T models.

Π-model



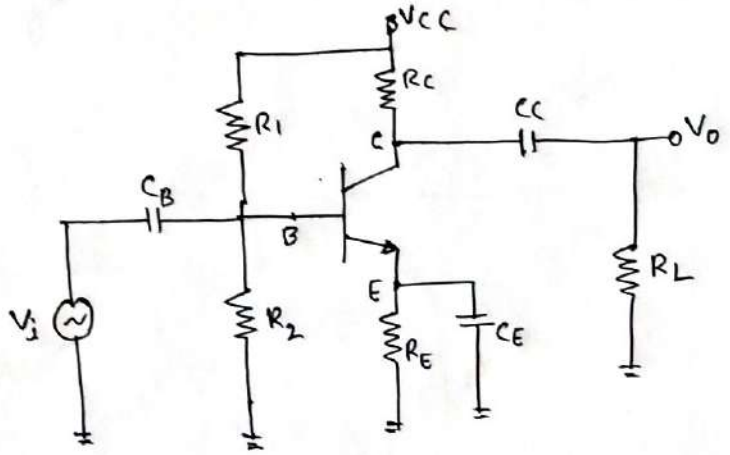
T-model



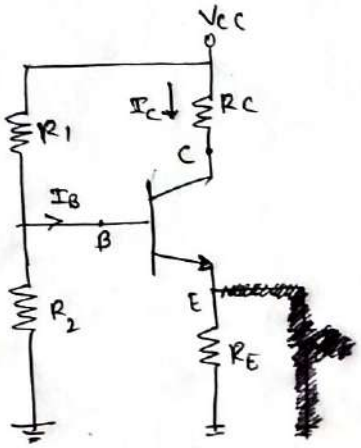
Using this circuit we can calculate input impedance, output impedance, voltage gain and current gain.

★ VDB Amplifier

The general VDB amplifier is given by

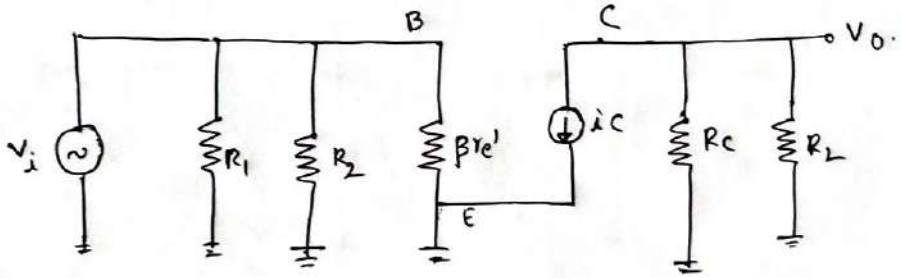


The DC equivalent circuit of VDB Amplifier is.

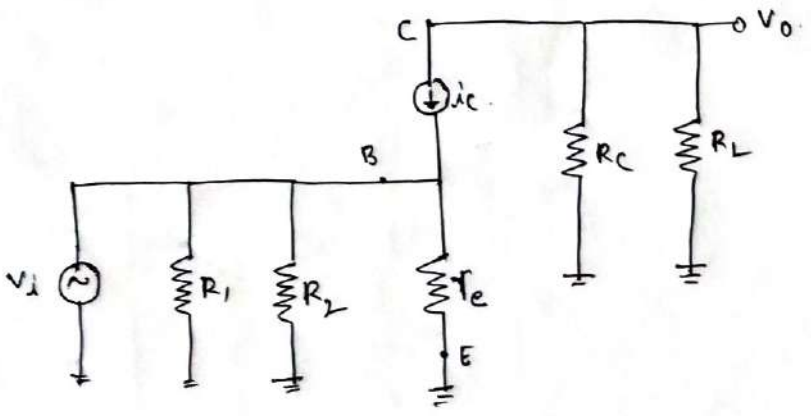


The AC equivalent circuit of VDB Amplifier is.

Π-model

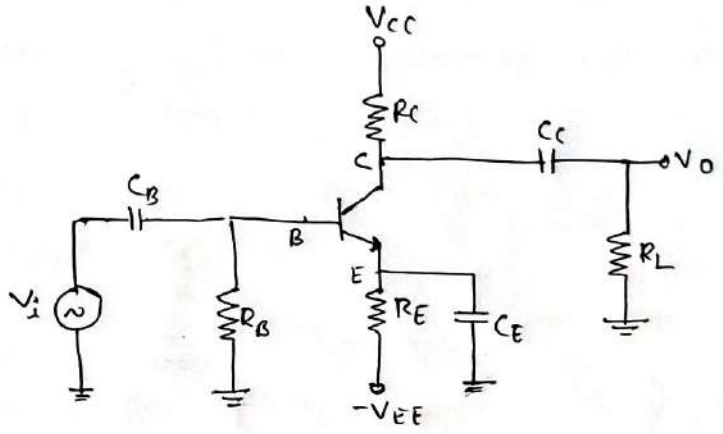


T-model

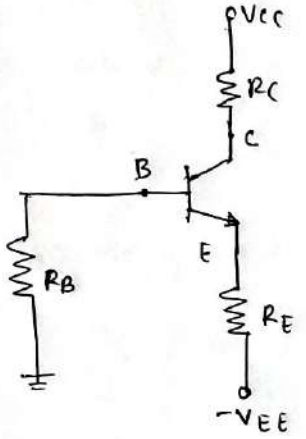


* TSEB Amplifer

The general circuit diagram of TSEB Amplifer is

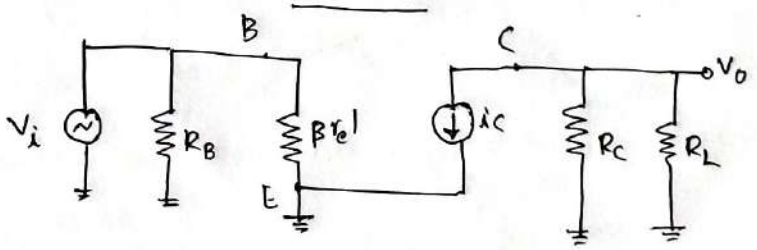


The DC equivalent circuit is given by

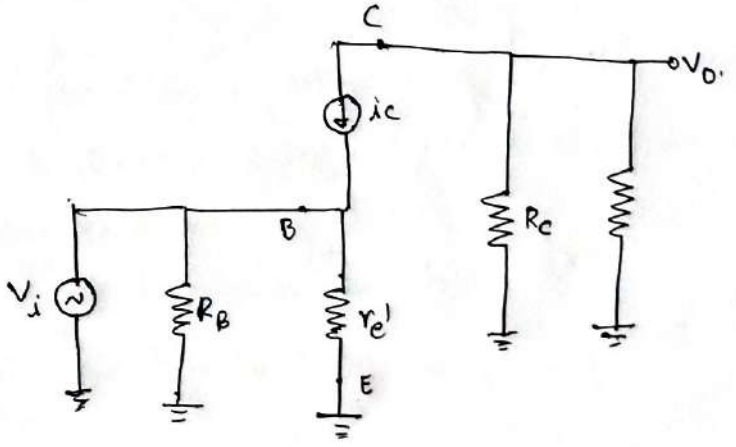


The Ac equivalent circuit is given by

TI-model



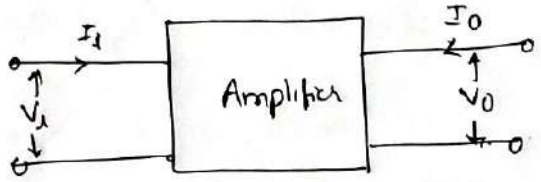
T model



H- Parameters

It is also called as Hybrid parameters.

Here voltage of input section and current of output section is expressed in terms of current of input section and voltage of output section.



* Let us consider the amplifier with V_i, V_o, I_i and I_o.

  Here I_i and V_o are Independent variables

  V_i and I_o are Dependent variables.

  we can write as $V_i = f_1(I_i, V_o)$

  $I_o = f_2(I_i, V_o)$

* In the equation form we can write as.

$$V_i = h_{11} I_i + h_{12} V_o \quad \text{— (1)}$$

$$I_o = h_{21} I_i + h_{22} V_o \quad \text{— (2)}$$

* In matrix form the above equations can be written as.

$$\begin{bmatrix} V_i \\ I_o \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_i \\ V_o \end{bmatrix}$$

* Assuming the short circuit condition of the output terminal, we get $V_o = 0$

  so $V_i = h_{11} I_i$ from eq (1).

$$h_{11} = \frac{V_i}{I_i} \Big|_{V_o = 0}$$

h_{11} is the ratio of input voltage to the input current when the output is short circuited. so it is called as Input Impedance. Expressed in ohms.

h_{11} is represented as h_i

For Common Emitter Transistor h_{ie}.

* From equation (2)

$$V_0 = 0$$

$$I_0 = h_{21} I_i$$

$$h_{21} = \frac{I_0}{I_i} \Big|_{V_0 = 0}$$

h_{21} is the ratio of output current to the input current when output port is short circuited. So it is called as Forward current gain.

h_{21} is represented as h_f

For CE configuration it is given as $\boxed{h_{fe}}$

* Assumming the open circuit condition of Input terminal, we get

$$I_i = 0$$

from equation (1)

$$V_i = h_{12} V_0$$

$$h_{12} = \frac{V_i}{V_0} \Big|_{I_i = 0}$$

h_{12} is the ratio of the input voltage to the output voltage when input section is open circuited. So it is called as Reverse voltage gain

h_{12} is represented as h_r.

For CE configuration, it is expressed as $\boxed{h_{re}}$

* From equation (2)

$$I_i = 0$$

$$I_0 = h_{22} V_2$$

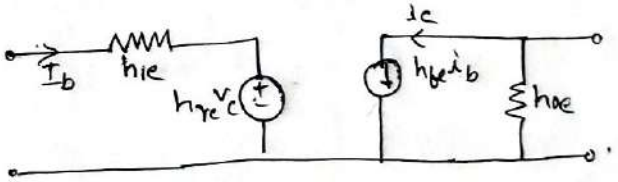
$$h_{22} = \frac{I_0}{V_2} \Big|_{I_i = 0}$$

h_{22} is the ratio of output current to the output voltage. when input section is open circuited. So it is called as output Admittance.

h_{22} is represented as h_o.

For CE configuration, it is expressed as $\boxed{h_{oe}}$

* The Hybrid equivalent circuit is given as.



r-parameters

There are mainly 5 r-parameters of a BJT. $\alpha, \beta, r_e', r_b'$ & r_c'

The relationship of h-parameter and r-parameters is given by

$$\alpha = h_{fb}$$

$$\beta = h_{fe}.$$

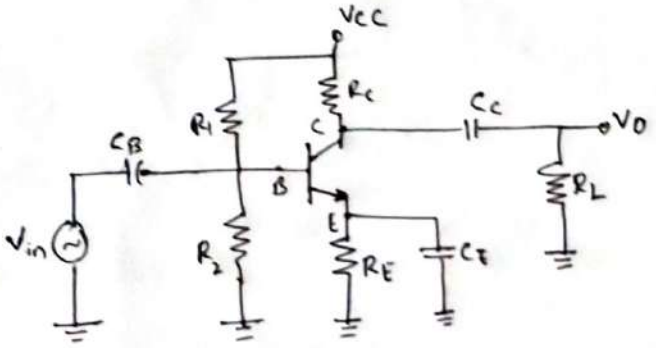
$$r_e' = \frac{h_{ie}}{h_{oe}}$$

$$r_c' = \frac{(1+h_{re})}{h_{oe}}$$

$$r_b' = \frac{h_{ie} - h_{re}}{h_{oe}(1+h_{fe})}.$$

Voltage Amplifiers

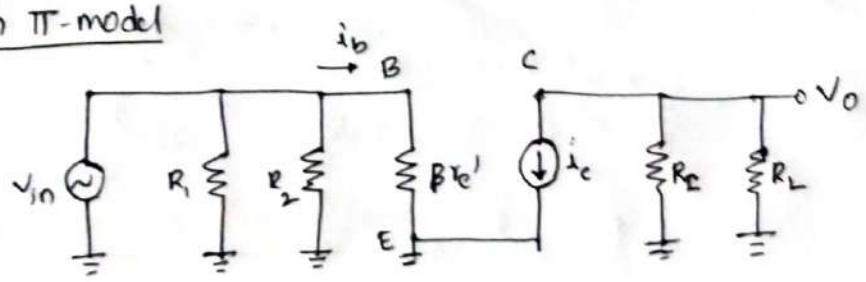
For Analysis of voltage Amplifers we are considering VDB Amplifier.



Voltage gain is defined as the Ac output voltage divided by Ac input voltage.

$$A_V = \frac{V_o}{V_{in}}.$$

From π-model



The Ac base current i_b flows through the input impedance of the base. so $V_{in} = i_b (R_1 \| R_2 \| \beta r_e')$

The Ac collector current i_c flows through the collector terminal

$$V_o = i_c (R_c \| R_L) = \beta i_b (R_c \| R_L)$$

$$A_V = \frac{V_o}{V_{in}} = \frac{\beta i_b (R_C \| R_L)}{i_b (R_1 \| R_2 \| \beta r_e')}$$

$$A_V = \frac{\beta \cdot (R_C \| R_L)}{(R_1 \| R_2 \| \beta r_e')}$$

Considering R_1 & R_2 are very high compared to r_e'

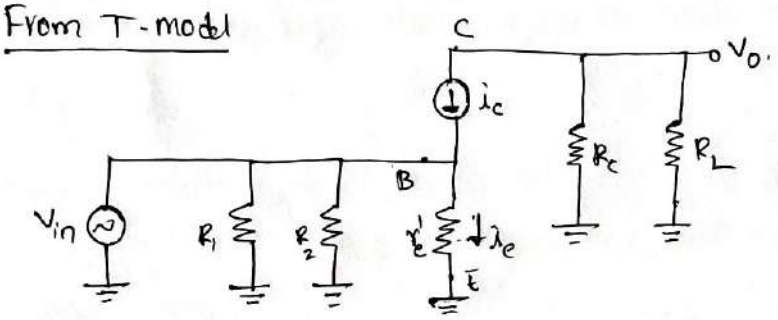
$$R_1 \| R_2 \| \beta r_e' \simeq \beta r_e'$$

$$A_V = \frac{\beta (R_C \| R_L)}{\beta r_e'} = \frac{R_C \| R_L}{r_e'}$$

Considering $r_c = R_C \| R_L$

$$\boxed{A_V = \frac{r_c}{r_e'}}$$

From T-model



The input voltage V_{in} is appearing across r_e'. we can write as

$$V_{in} = [redacted] i_e r_e'$$

The Ac collector current i_c flows through the output terminal.

$$V_o = i_c (R_C \| R_L) = i_e r_c$$

Voltage gain $A_V = \frac{i_c r_c}{i_e r_e'}$

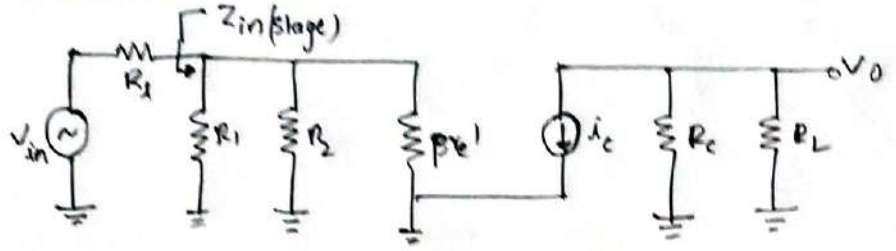
$i_c \simeq i_e \Rightarrow$ $\boxed{A_V = \frac{r_c}{r_e'}}$

Loading effect of Input Impedance

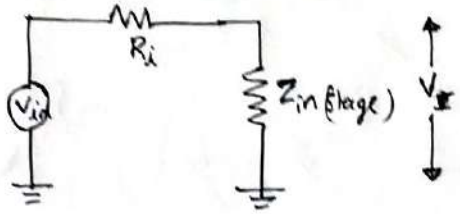
The Ac voltage source has an internal resistance of R_i.
When the Ac signal is not stiff. Some of the Ac voltage is dropped across it internal resistance. So the Ac voltage between the base and ground is less than ideal.

The Ac generator has to drive the input impedance of the stage

$Z_{in(stage)}$.



$$Z_{in(stage)} = R_1 \| R_2 \| \beta r_e'$$



When the generator is not stiff, the AC input voltage V_I is less than V_{in}.

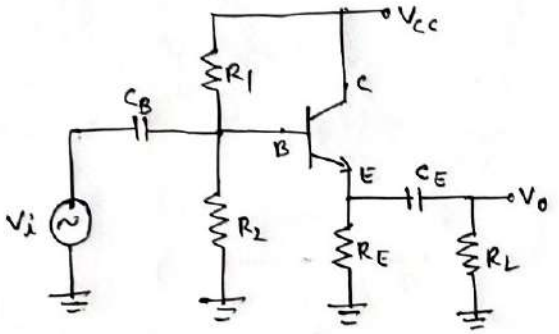
$$V_I = \frac{Z_{in(stage)}}{R_i + Z_{in(stage)}} V_{in}$$

The generator is stiff when R_i is less than $0.01\, Z_{in(stage)}$.

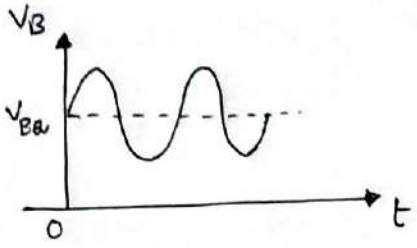
CC Amplifier

Common collector Amplifier is also called as Emitter Follower. The input signal is applied to the base and output signal is taken from the emitter.

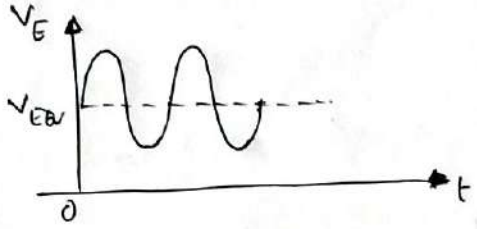
The circuit of cc amplifier is given as



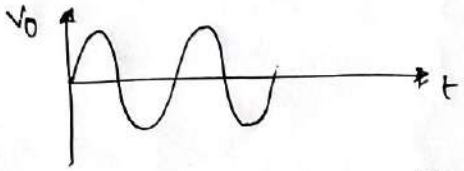
* Here the collector is at ac ground. The input voltage is applied to the base. It produces an ac emitter current and produces an ac voltage across the emitter resistor.
* This AC voltage is applied to the load resistor.
* The input voltage is applied between base and ground. This voltage has a DC component and an AC component. This voltage rides on the quiescent base voltage V_{BQ}.



* A voltage is developed across emitter resistor and it is centered on a quiescent emitter voltage V_{EQ}. This waveform is given as



* The AC emitter voltage flows through coupling capacitor C_E, so the output voltage across load resistor is pure AC signal and it is inphase with input signal.

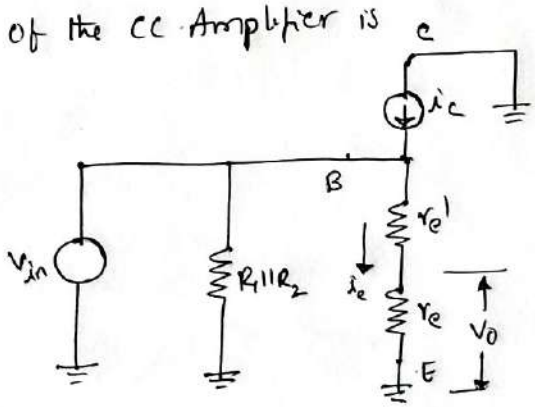


* Since the output voltage is following the input voltage, this circuit is called as Emitter follower.

* The AC Emitter resistance is given from the circuit as

$$r_e = R_E \parallel R_L$$

The T-model of the CC Amplifier is



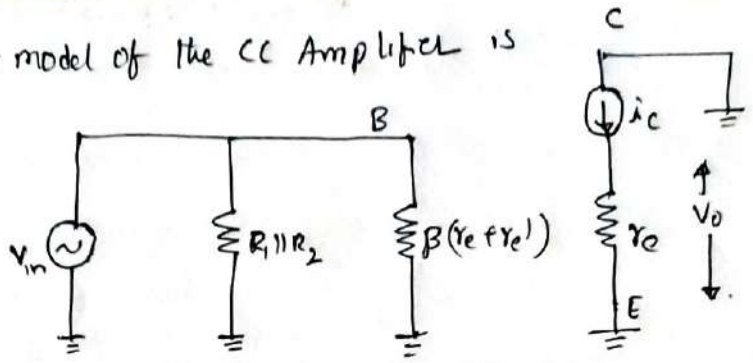
Here $V_0 = i_e r_e$

$$V_{in} = i_e (r_e + r_e')$$

$$A_V = \frac{V_0}{V_{in}} = \frac{r_e}{r_e + r_e'}$$

Generally $r_e >> r_e'$ so $A_V \simeq 1$

The π- model of the CC Amplifier is



The input impedance of the Base is given as

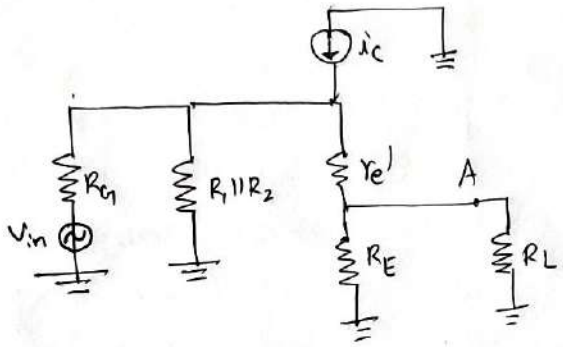
$$Z_{in(Base)} = \beta(r_e + r_e')$$

The input impedance of the amplifier is given as

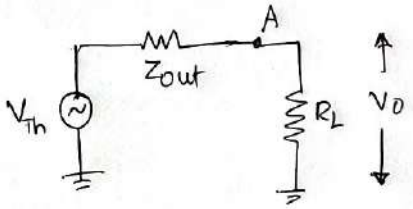
$$Z_{in(stage)} = R_1 \| R_2 \| \beta(r_e + r_e').$$

Output impedance

The AC equivalent circuit of an Emitter follower is given as



Applying Thevenin's theorem at output point 'A'.



$$Z_{out} = R_E \| \left(r_e' + \frac{R_G \| R_1 \| R_2}{\beta} \right).$$

The impedance of the base circuit is $R_G \| R_1 \| R_2$.

The current gain of the transistor gives this impedance by a factor β.

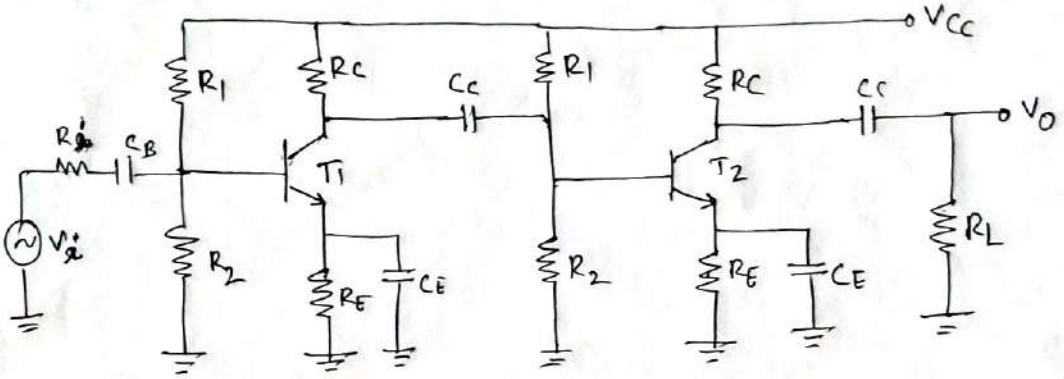
So the impedance value is reduced.

We are selecting the load resistor and other resistor so that for a stiff voltage source $Z_{out} << R_L$.

The Emitter follower can deliver maximum power to a low impedance value.

Multistage Amplifiers

* A multistage amplifier is designed by cascading two or more amplifier stages. The output of the first stage is the input of the second stage.
* To get more voltage gain we are designing multistage amplifiers.
* The two stage amplifier is given by

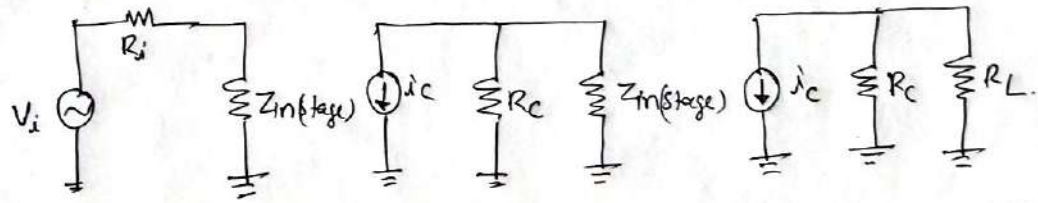


→ The amplified and inverted signal of first stage is coupled to base of the second stage.

→ The amplified and inverted output of second stage is then coupled to the load resistor.

→ The signal across load resistor is in phase with input signal.

* The AC equivalent circuit is given by.



→ The Z_{in} of the second stage is in parallel to R_C of first stage.

The AC collector resistance of first stage is.

$$r_c = R_C \,||\, Z_{in(stage)}$$

→ The voltage gain of first stage is $A_{V_1} = \dfrac{R_C \,||\, Z_{in(stage)}}{r_e'}$

→ The AC collector resistance of second stage is

$$r_c = R_C \,||\, R_L$$

→ The voltage gain of second stage is $A_{V_2} = \dfrac{R_C \,||\, R_L}{r_e'}$

→ The total voltage gain is given by $A_V = (A_{V_1}) \cdot (A_{V_2})$