



AKSHAYA INSTITUTE OF TECHNOLOGY

Approved by AICTE, New Delhi, Affiliated to VTU, Belgaum, Recognized by Govt. of Karnataka,

Obalapura Post, Lingapura, Koratagere Road, Tumkur - 572 106, Karnataka



DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Module 1 Notes for “VLSI Design and Testing” [BEC602]

Prepared by:

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Lingapura, Obalapura Post, Koratagere Road, Tumakuru - 572106

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



VISION

To produce competent engineering professionals in the field of Electronics and Communication Engineering by imparting value based quality technical education to meet the societal needs and to develop socially responsible citizens.



MISSION

M1: To provide strong fundamentals and technical skills in the field of Electronics and Communication Engineering through effective teaching learning process.

M2: Enhancing employability of the students by providing skills in the fields of VLSI, Embedded systems, Signal processing, etc., through Centre of Excellence.

M3: Encourage the students to participate in co-curricular and extra-curricular activities that creates a spirit of social responsibility and leadership qualities.



Program Specific Outcomes (PSOs)

After Successful Completion of Electronics and Communication Engineering Program Students will be able to

1. Apply fundamental knowledge of core. Electronics and Communication Engineering in the analysis, design and development of Electronics Systems as well as to interpret and synthesize experimental data leading to valid conclusions.
2. Exhibit the skills gathered to analyze, design, develop software applications and hardware products in the field of embedded systems and allied areas.



Program Educational Objectives (PEOs)

PEO1: Graduates exhibit their innovative ideas and management skills to meet the day to day technical challenges.

PEO2: Graduates utilize their knowledge and skills for the development of optimal solutions to the problems in the field of Electronics and Communication Engineering..

PEO3: Graduates exhibit good interpersonal skills, leadership qualities and adapt themselves for life-long Learning



VLSI Design and Testing		Semester	6
Course Code	BEC602	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		
<p>Course objectives:</p> <ol style="list-style-type: none"> 1. This course deals with analysis and design of digital CMOS integrated circuits. 2. The course emphasizes on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology. 3. This course will also cover switching characteristics of digital circuits along with delay and power estimation. 4. Understanding the CMOS sequential circuits and memory design concepts. 5. Explore the knowledge of VLSI Design flow and Testing. 			
<p>Teaching-Learning Process (General Instructions)</p> <p>These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.</p> <ol style="list-style-type: none"> 1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes. 2. Show Video/animation films to explain the different concepts of Digital Signal Processing 3. Encourage collaborative (Group) Learning in the class 4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking 5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it. 6. Topics will be introduced in a multiple representation. 7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them. 8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding. 9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes. 			
MODULE-1			
<p>Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison. [Text 1: 1.1,1.2,1.3,1.4,1.5.1.6.]</p>			
<p>Teaching-Learning Process: Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2</p>			
MODULE-2			

MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence of β_n / β_p ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS. [Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.]

MODULE-3

CMOS Process Technology: Silicon Semiconductor Technology, CMOS Technologies, Layout Design Rules. [Text 1: 3.1,3.2,3.3.]

Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield. [Text 1: 4.1,4.2,4.3,4.4,4.5.4.6.4.7,4.8,4.9,4.10]

Teaching-Learning Process:

Chalk and talk method/Power point presentation, YouTube Videos RBT Level: L1, L2, L3.

MODULE-4

CMOS Circuit and Logic Design: Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads. [Text 1: 5.1,5.2,5.2.1, , 5.2.2, 5.2.3, 5.2.4, 5.2.6, 5.2.8, 5.3,5.3.1,5.3.2, 5.3.4 ,5.3.8,5.5]

Teaching-Learning Process:

Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3.

MODULE-5

Sequential MOS Logic Circuits: Introduction, Behaviour of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch.[Text2: 8.1, 8.2, 8.3, 8.4]

Structured Design and Testing: Introduction, Design Styles, Testing[Text1: 6.1, 6.2. 6.5]

Teaching-Learning Process:

Chalk and talk method/Power point presentation RBT Level: L1, L2, L3

Text Books:

1. Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company.
2. “CMOS Digital Integrated Circuits: Analysis and Design”, Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.

Reference Books:

1. “CMOS VLSI Design- A Circuits and Systems Perspective”, Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.
2. “Basic VLSI Design”, Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors
CO2	Design and realize combinational, sequential digital circuits and memory cells in CMOS logic.
CO3	Analyze the synchronous timing metrics for sequential designs and structured design basics.
CO4	Understand designing digital blocks with design constraints such as propagation delay and dynamic power dissipation.
CO5	Understand the concepts of Sequential circuits design and VLSI testing

Module - 1

Introduction to CMOS circuits

• Generation of IC's

Year	Generation	No. of transistors	Examples.
1961	SSI	10 - 100	Logic gates, FF
1966	MSI	100 - 1000	Adders, MUX, counters
1971	LSI	1000 - 10000	8 bit μ p's, RAM, ROM
1980	VLSI	10000 - 1 million	16 & 32 bit μ p's, DRA
1990	ULSI	1m - 10 million	DSD's, Smart sensors
2000	ESI	> 10 m	ASIC's, SOC

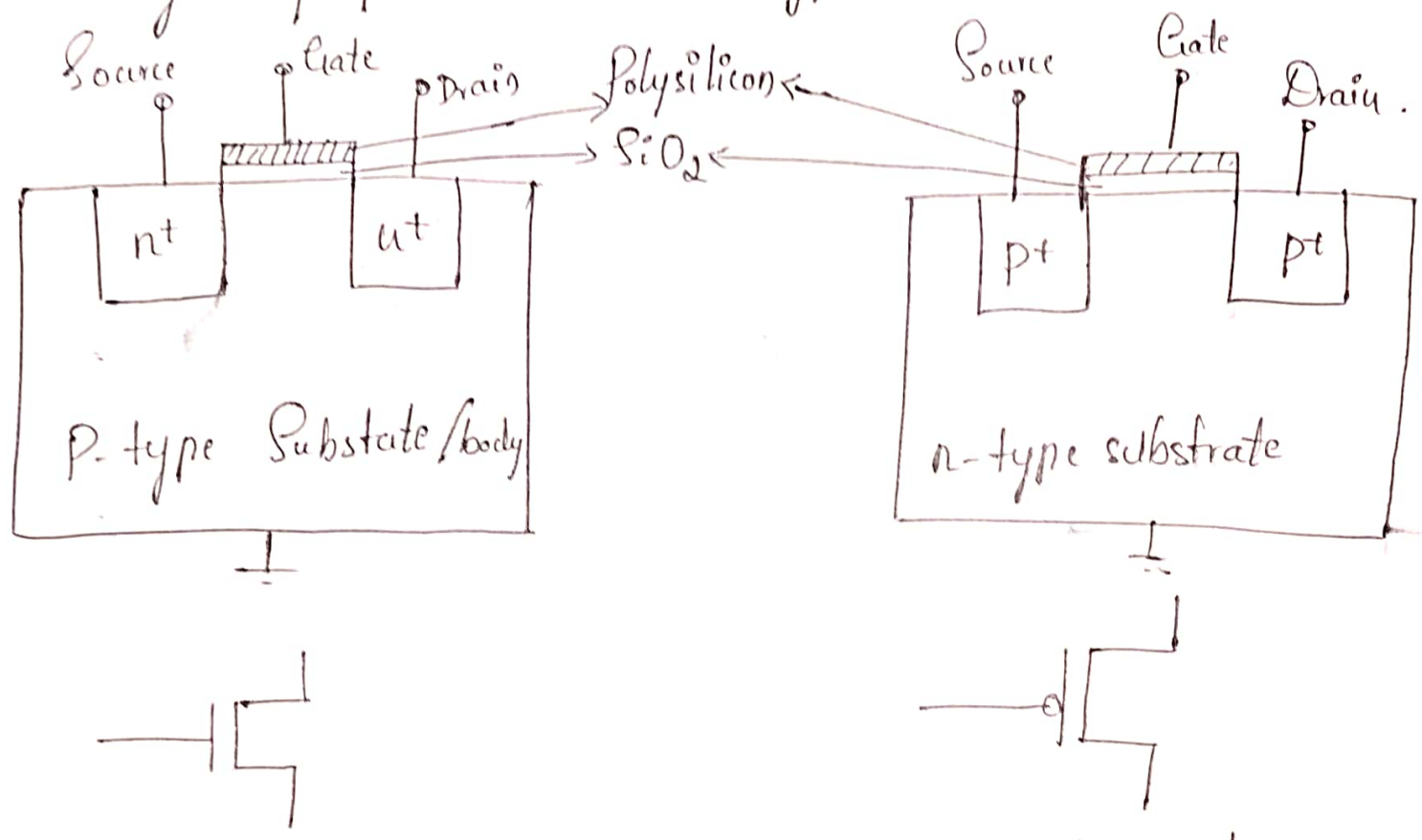
Moore's law : (Gordon Moore, 1965)

"The number of transistors integrated on IC doubles for every 18 months"

Truly the 1970's, 80's, 90s may be regarded as integrated circuit era.

• MOS Transistors (Metal oxide semiconductor/silicon)
MOS transistor are created by superimposing several layers of conducting and insulating materials to form a sandwich like structure.

CMOS technology provides two types of transistor as n-type and p-type transistors. Transistor operation is based on electric fields hence they are called as field effect transistor. cross section and symbols of these transistor are shown the nt and pt regions indicate heavily doped n or p-type silicon.



Nmos transistor
 An nmos transistor is built with a p-type body and has region of n-type semiconductor adjacent to gate called the source and drain, they are physically equivalent and interchangeable. The body is typically grounded.

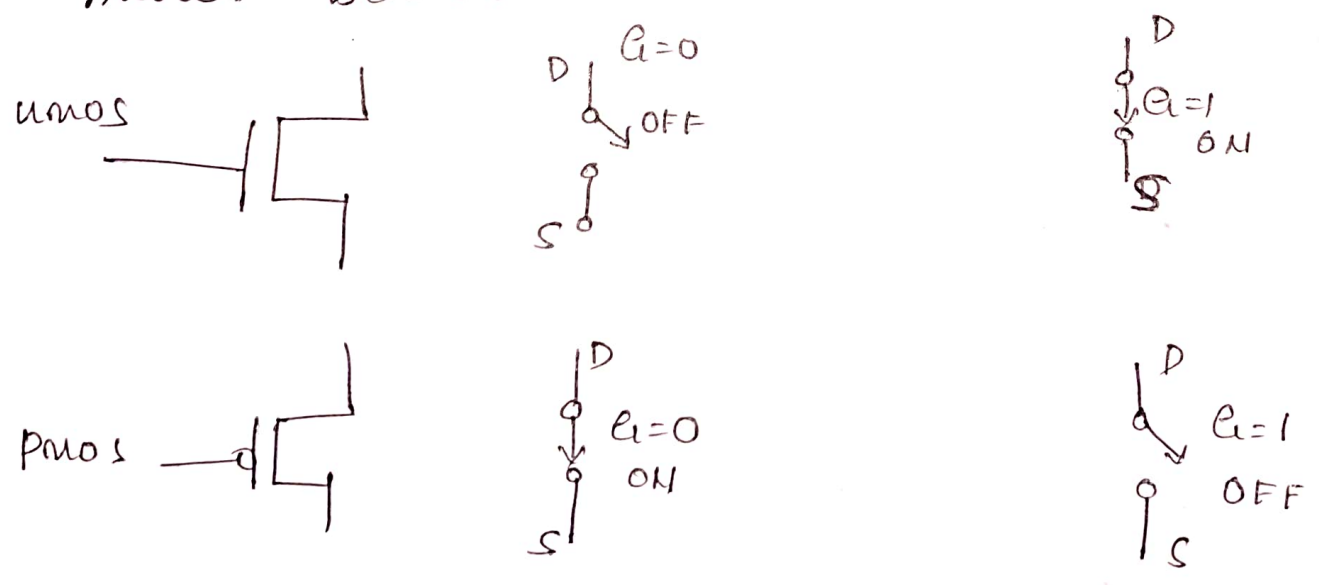
PMOS transistor
 A PMOS transistor is built with an n-type body and has region of p-type semiconductor adjacent to gate called the source and drain, they are physically equivalent and interchangeable. The body is typically grounded.

nmos transistor can pass good 0's and poor 1's.
 A pmos transistor is just opposite,
 contains P type source and drain region with
 n-type body.

For nmos a transistor when $g=0$ p-n
 junctions of the source and drain to body
 are reverse biased and transistor is OFF,
 when $g=1$ transistor is ON (logic 1) & (logic 0)

For pmos transistor when $g=0$ transistor
 is ON and when $g=1$, the transistor is OFF

The high potential is represented as V_{DD} or
 logic 1 (5V) and low potential as GND or
 V_{SS} a logic 0 (0V) The switch model is
 shown below.



Physical structure of MOS transistors.

(2)

INTRODUCTION TO CMOS CIRCUITS

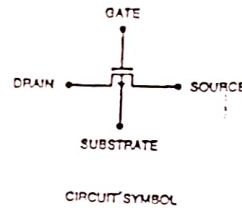
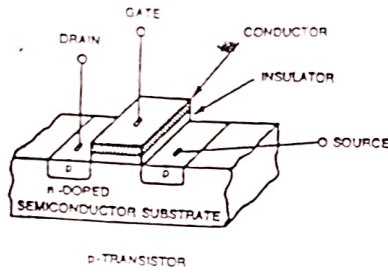
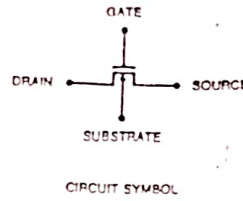
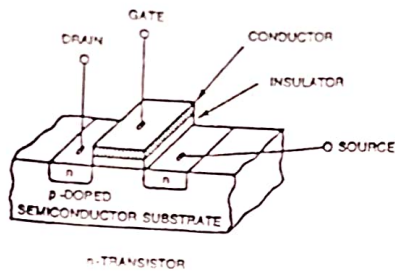


FIGURE 1.1. MOS transistor physical structures

• MOS transistor switches

The Gate controls the passage of current between the drain and source. and simplify the MOS transistors to be viewed as simple turn ON/OFF switches.

The strength of a signal is measured by its ability to sink or source current.

nmos switch / n switch

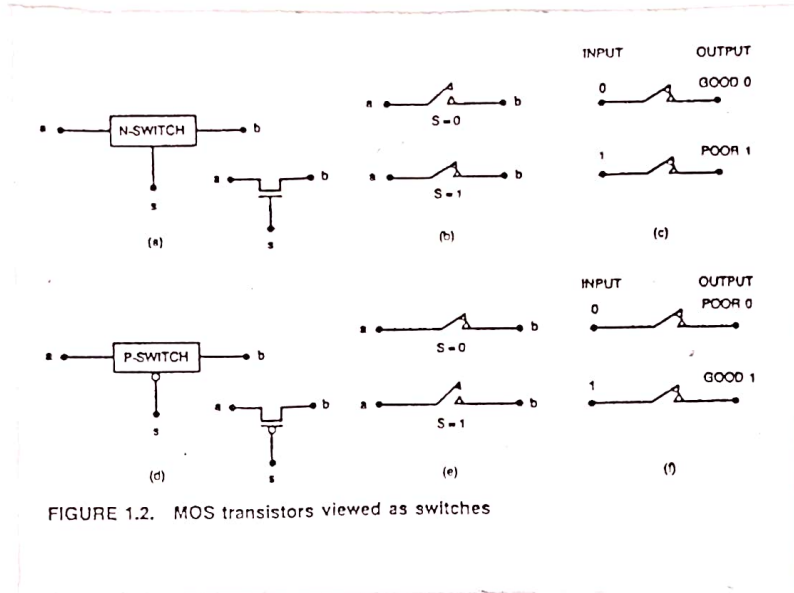
nmos transistors can pass good zeros and poor 1's.

GOOD 1 = 5V / Exact v_{tq}
POOR 1 = 4.9V / 4.8V / some vary.

CMOS Switches / P Switches

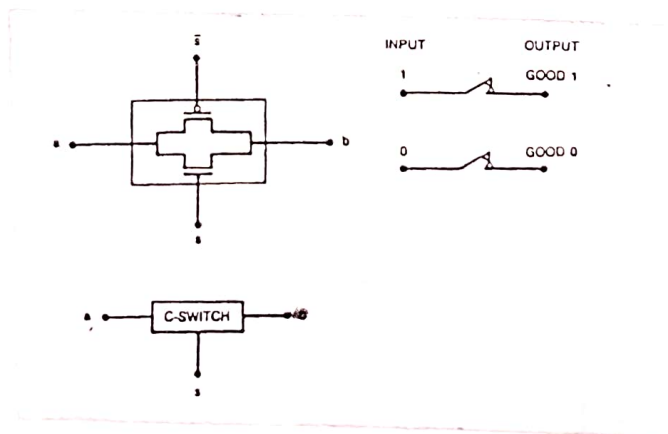
PMOS transistors can pass GOOD 1's and POOR 0's.

The representation n-switch and P-switch is as shown below.



C-Switch (Complementary switch/Transmission gate)

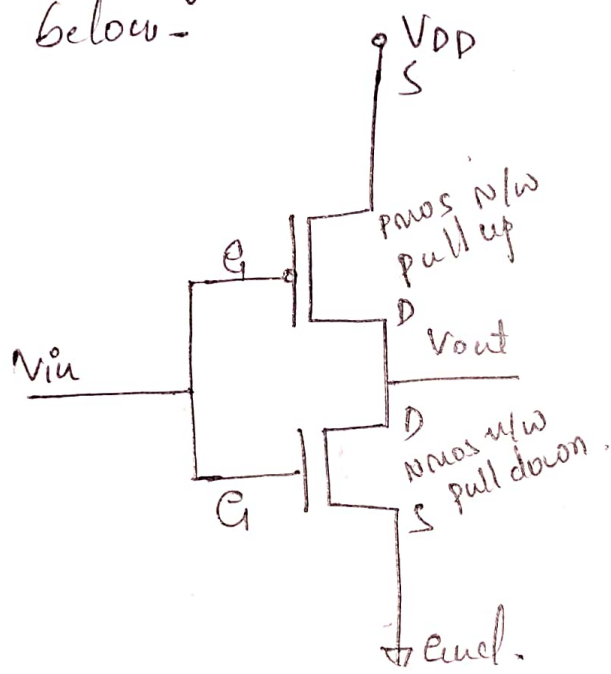
It is an combination of PMOS & NMOS
So it can pass GOOD 0's and GOOD 1's.



CMOS Logic Inverter

A CMOS inverter is a fundamental logic gate that inverts a digital signal, using a pair of complementary transistors (One N-type & One P-type MOSFET) to efficiently switch between logic states (high and low).

The CMOS logic inverter is represented as shown below -



Input	Output
1	0
0	1

Note :

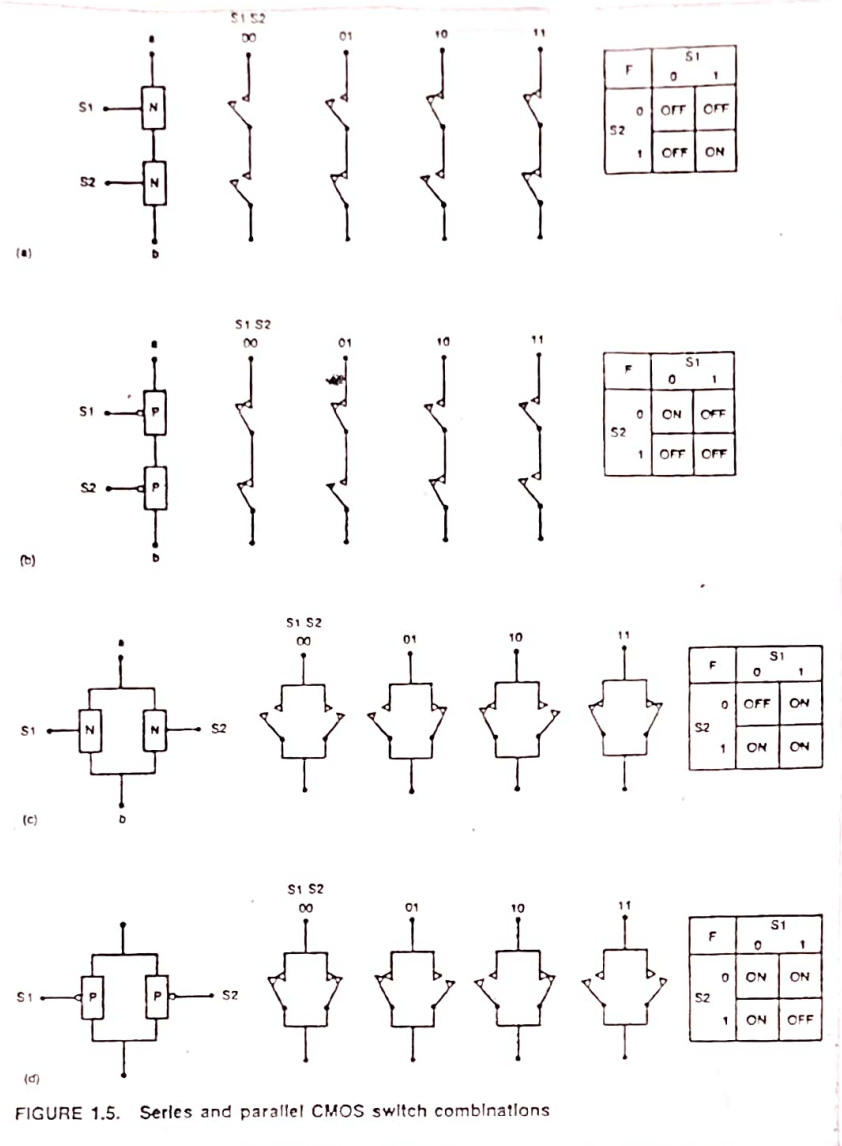
For N-Switch \rightarrow in series connection it yields AND function $(A \cdot B)$

* in parallel \rightarrow OR $(A + B)$

For P-Switch \rightarrow in series \rightarrow OR $(A + B)$

in parallel \rightarrow AND $(A \cdot B)$

WOL



What is CMOS?

- Complementary metal-oxide silicon
- Uses both NMOS and PMOS transistors to implement logic function

Advantages

- Low power consumption (no current flow when stable state)
- High noise immunity
- Scalability and integration.

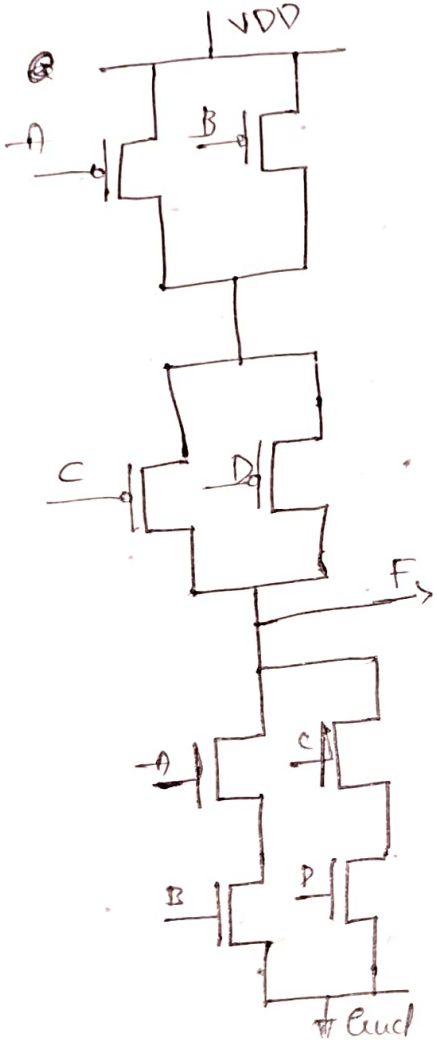
basic gates in CMOS: NOT, AND, OR, NAND, NOR, XOR, XNOR

Compound Gates

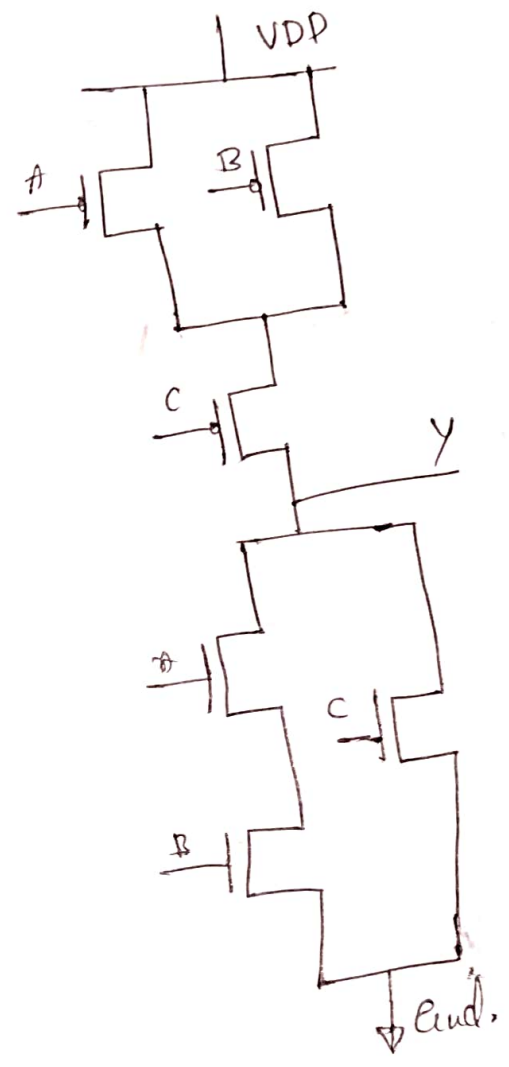
Construction for functions,

a) $F = \overline{AB+CD}$

b) $Y = \overline{AB+C}$



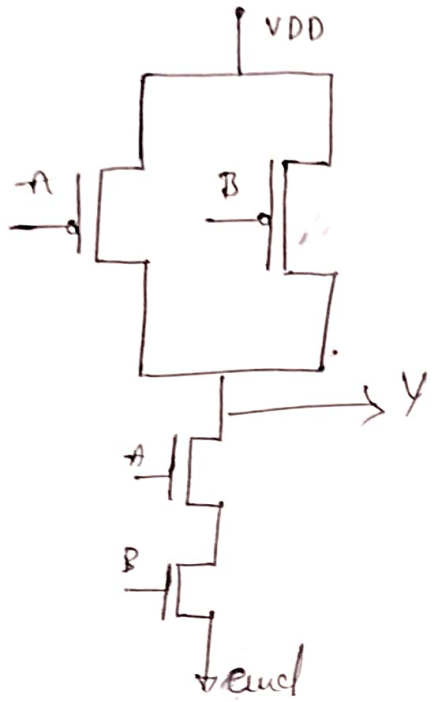
a) $F = \overline{AB+CD}$



b) $Y = \overline{AB+C}$

• Implement CMOS Structure for NAND function and NOR function

(a) $Y = \overline{A \cdot B}$

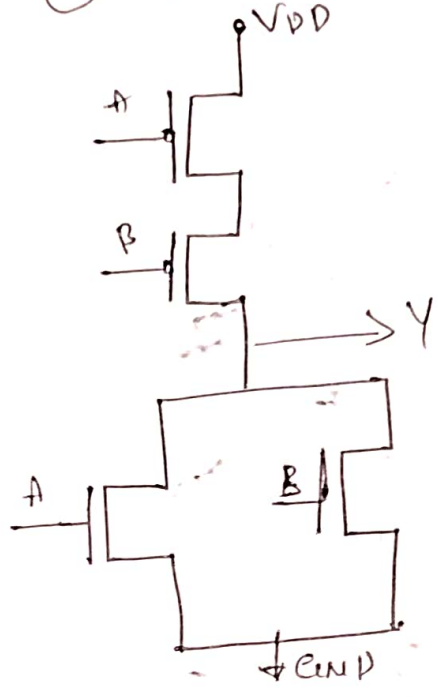


Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(a) NAND

(b) $Y = \overline{A + B}$



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

(b) NOR

A CMOS 2 to 1 multiplexer

(6)

A

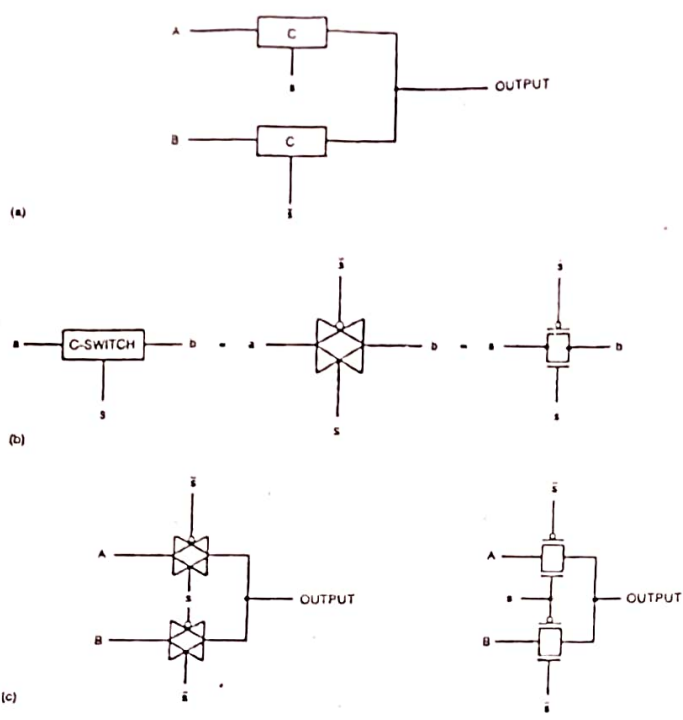


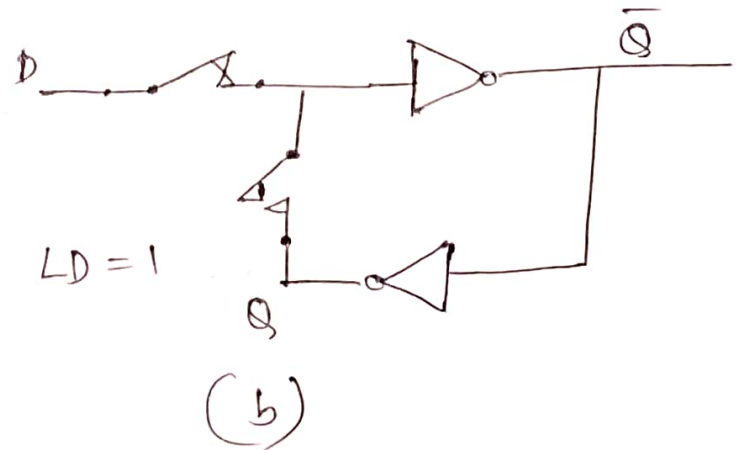
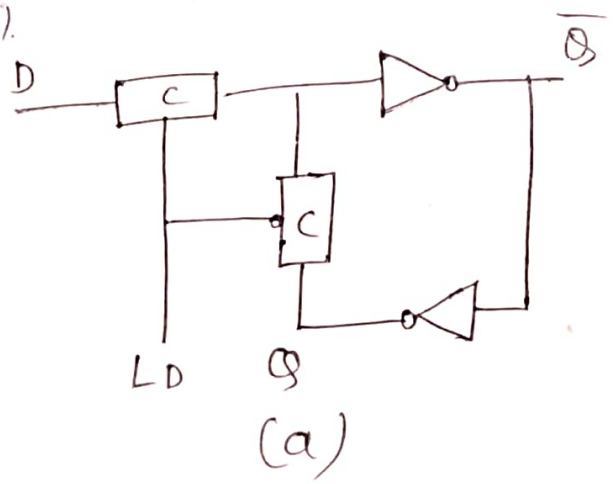
FIGURE 1.10. A CMOS 2-input multiplexer

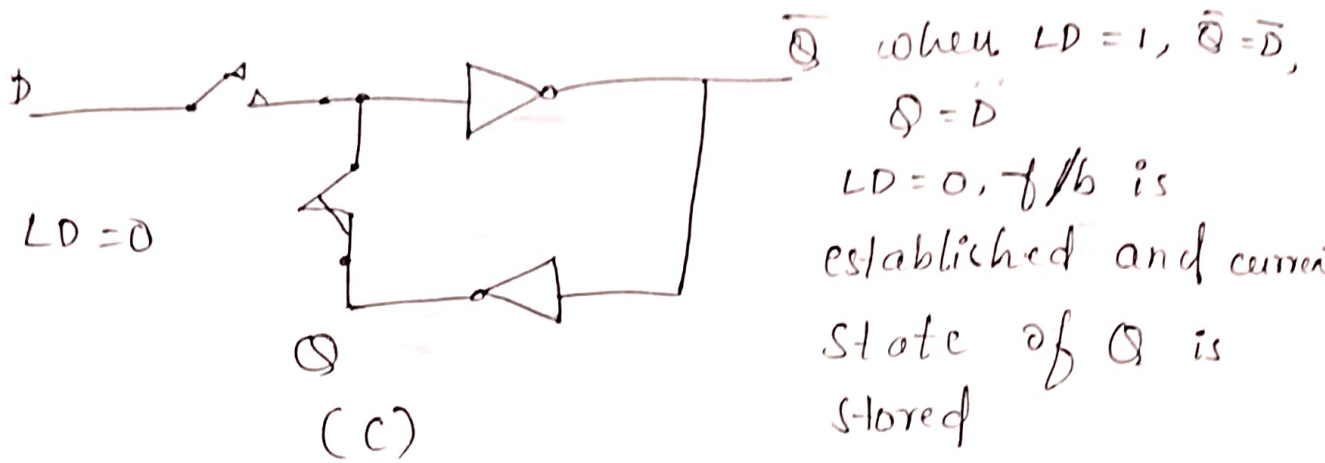
Memory :

Truth Table

A	B	S	\bar{S}	output
X	0	0	1	0 (B)
X	1	0	1	1 (B)
0	X	1	0	0 (A)
1	X	1	0	1 (A)

Representation of Simple CMOS flipflop





Alternate circuit representation

There are 3 types of circuit representation.

- Behavioural representation
- Structural representation.
- Physical representation

Behavioural representation

It describes how a particular design should respond to given set of inputs. It defines in terms of boolean function

$$\text{Ex: } F = \overline{(A+B+C) \cdot D}$$

$$S = a + b$$

$$Y = \overline{AB + CD}$$

Structural representation.

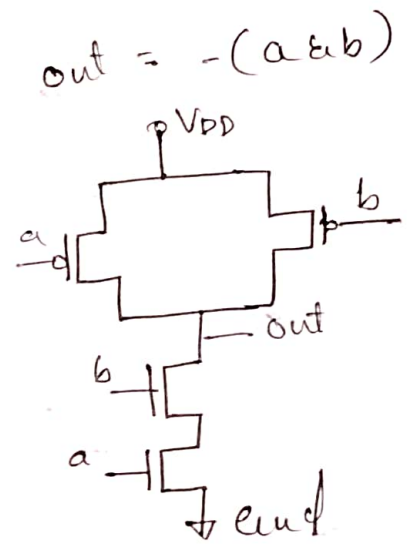
It specifies how components are interconnected to perform function.

Ex: * 2 input NAND gate (behavioural description)

" Part nand2 (a, b) → out
Signal ?!

- Nfet ?! a vss
- Nfet out b ?!
- Pfet out a vdd
- Pfet out b vdd "

End



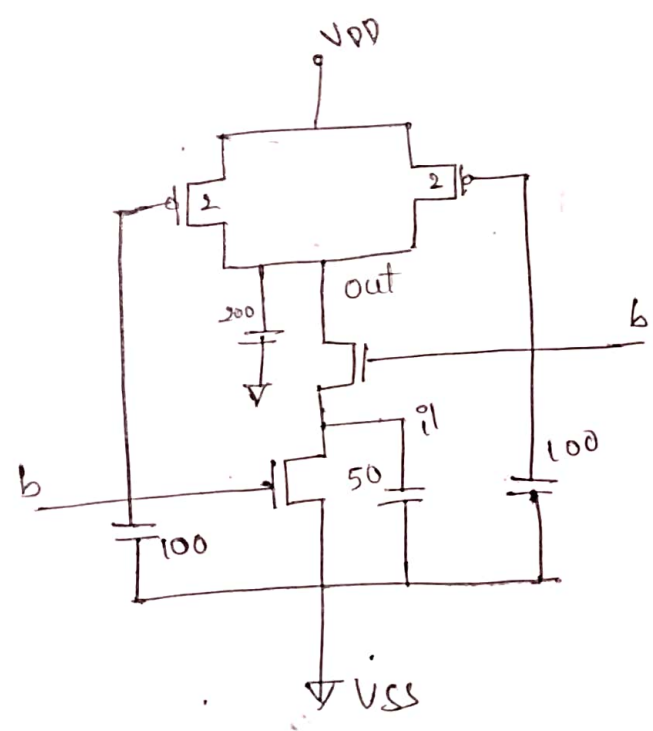
* 2 input NAND gate - Structural description

Part nand2 (a, b) → out

Signal ?!

- Nfet ?! a vss
- Nfet out a ?!
- Pfet out a vdd size = 2
- Pfet out b vdd size = 2

- capacitance ?! 50
 - capacitance a 100
 - capacitance b 100
 - capacitance out 200
- End



* Flipflop

Part of flipflop (in, ld, ldbar, q, qbar)

Signal a

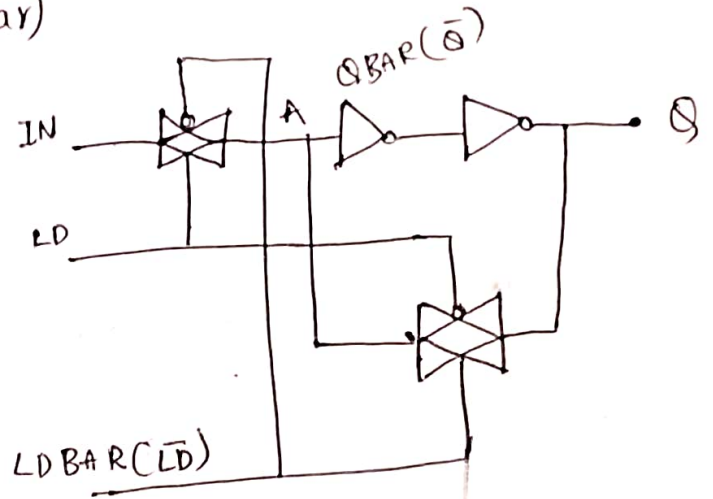
$$tq(in, ld, ldbar) \rightarrow a$$

$$inv(a) \rightarrow qbar$$

$$inv(qbar) \rightarrow q$$

$$tq(q, ldbar, ld) \rightarrow a$$

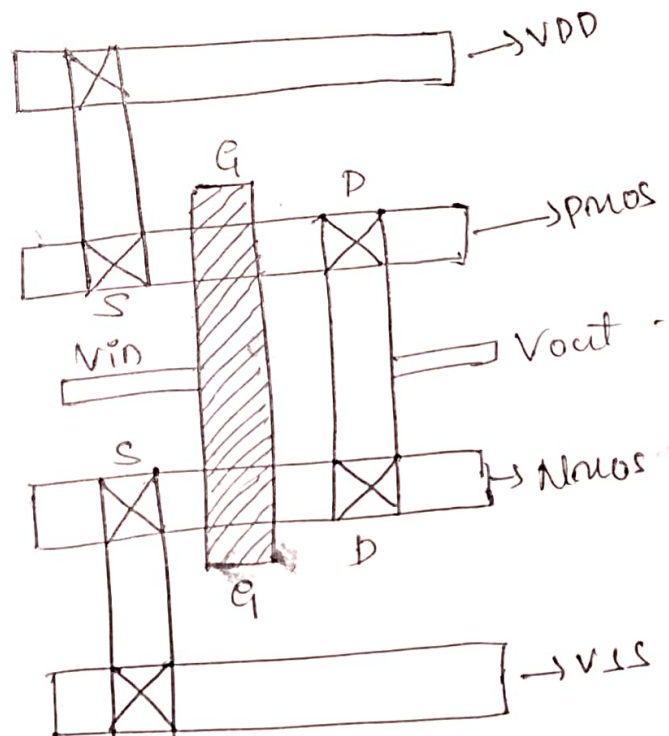
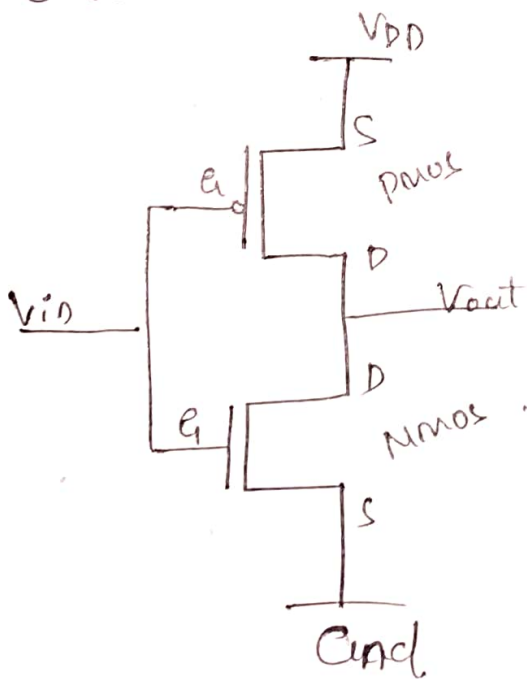
End



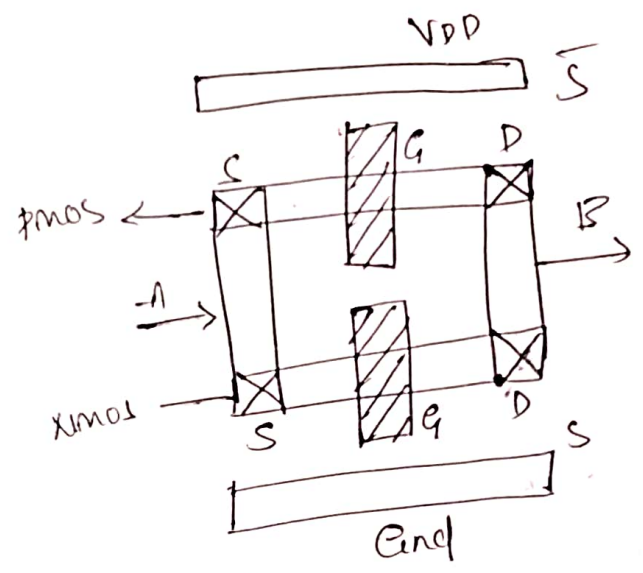
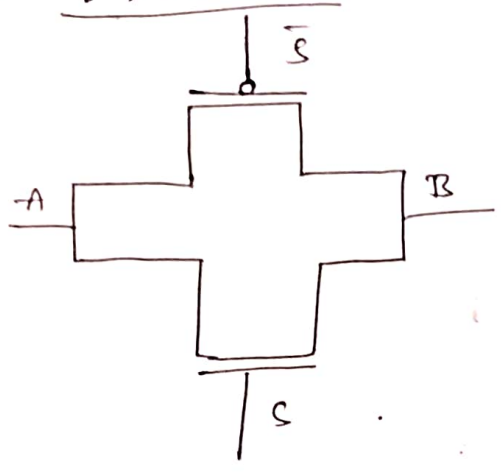
Physical representation

It is used to define how the particular part has to be constructed to yield a specific structure and hence behaviour.

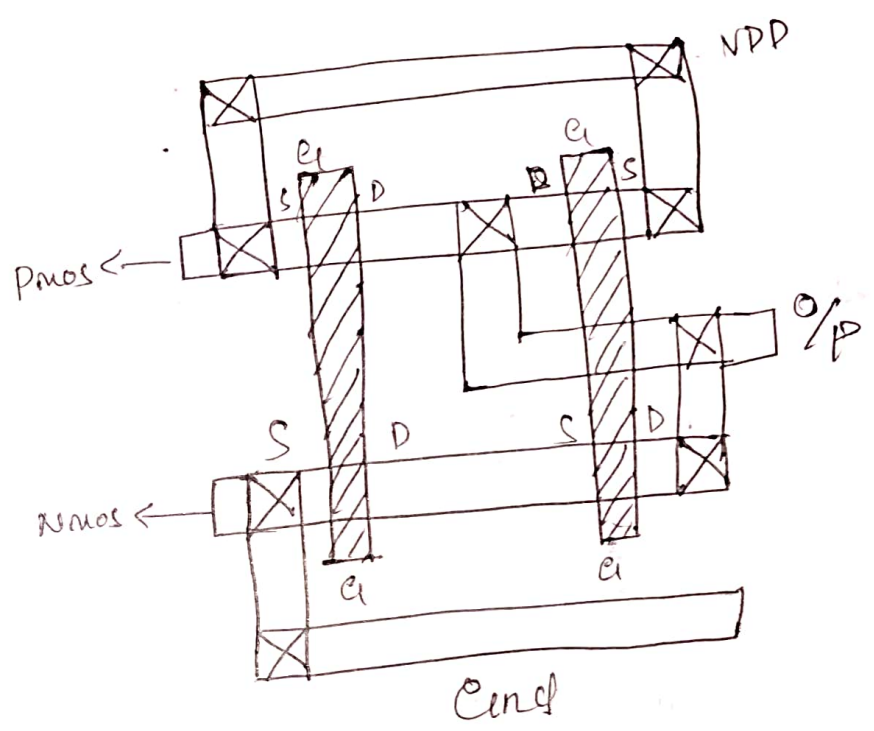
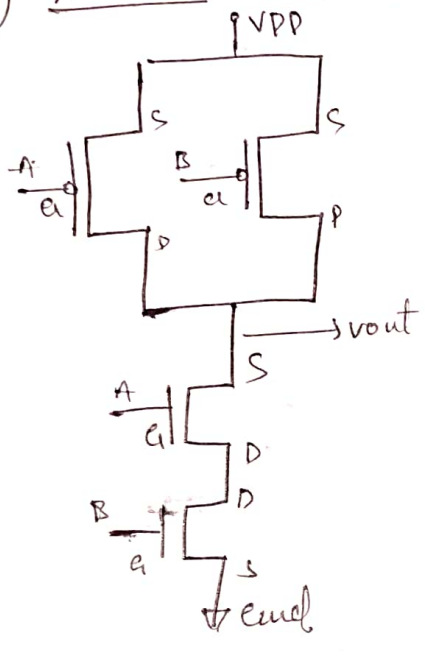
Ex
① CMOS Inverter



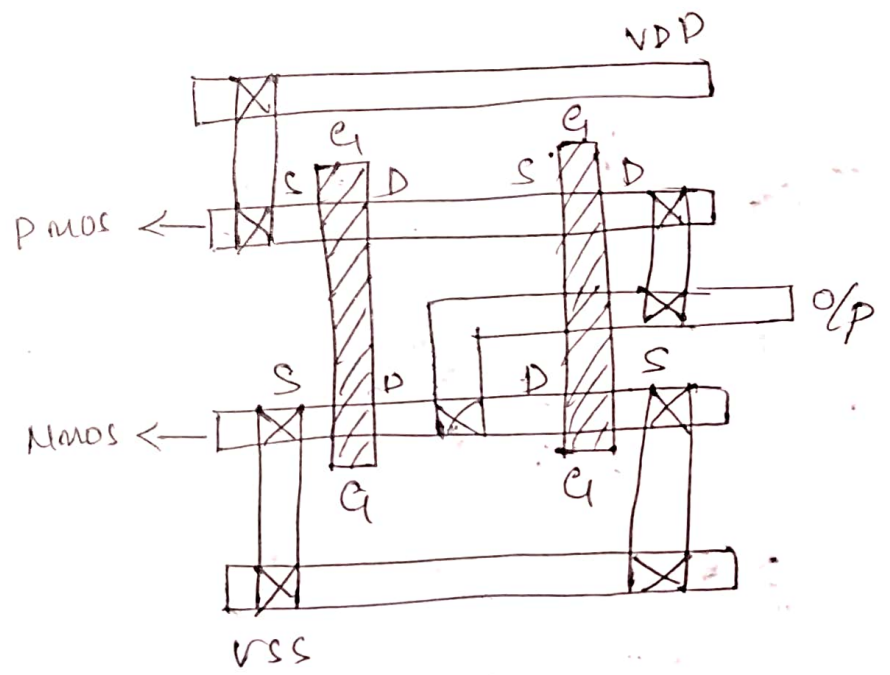
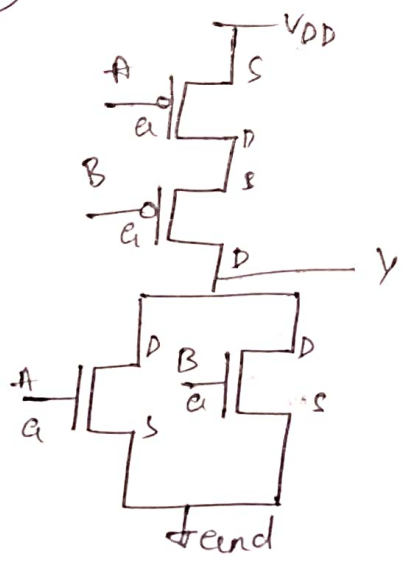
(b) Transmission Gates



(c) NAND Gate



(d) NOR Gate



Difference between CMOS and NMOS

⑨

Feature	CMOS	NMOS
Logic levels	<ul style="list-style-type: none">Fully restored logic, output settles at V_{DD} or V_{SS}	<ul style="list-style-type: none">Output does not settle at V_{SS} hence degraded noise margin
Transition times	<ul style="list-style-type: none">Rise & fall times are of the same order	<ul style="list-style-type: none">Rise times are inherently slower than fall times
Power dissipation	<ul style="list-style-type: none">Almost zero (except during switching)	<ul style="list-style-type: none">Higher (due to static current flow)
Precharging characteristics	<ul style="list-style-type: none">Both n-type & p-type devices are available for precharging a bus to V_{DD} and V_{SS}.	<ul style="list-style-type: none">with enhancement mode transistor the best one can do is to charge a bus to $(V_{DD} - V_t)$.
Power Supply	<ul style="list-style-type: none">Voltage required to switch a gate is fixed percentage of V_{DD}	<ul style="list-style-type: none">Somewhat dependent on supply voltage

Packing density

Pull-up and Pull-down Ratio

Layout

Variable range
1.5 to 15 volts.

- Require $2N$ devices for N inputs for complementary static gates. less for dynamic gates

Load-to-device ratio is typically 1:1 or 2:1

CMS encourages regular styles

Fixed.

- Require $(N+1)$ devices for N inputs.

load-to-device ratio is typically 4:1

Depletion load and different driver transistor sizes inhibit layout regularity