AKSHAYA INSTITUTE OF TECHNOLOGY

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Obalapura Post, Lingapura, Koratagere Road, Tumkur - 572 106, Karnataka

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Module 2 Notes for

"VLSI Design and Testing"

[BEC602]

Prepared by:

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

To produce competent engineering professionals in the field of Electronics and Communication Engineering by imparting value based quality technical education to meet the societal needs and to develop socially responsible citizens.

MISSION

M1: To provide strong fundamentals and technical skills in the field of Electronics and Communication Engineering through effective teaching learning process.

M2: Enhancing employability of the students by providing skills in the fields of VLSI, Embedded systems, Signal processing, etc., through Centre of Excellence.

M3: Encourage the students to participate in co-curricular and extra-curricular activities that creates a spirit of social responsibility and leadership qualities.

Program Specific Outcomes (PSOs)

After Successful Completion of Electronics and Communication Engineering Program Students will be able to

1. Apply fundamental knowledge of core. Electronics and Communication Engineering in the analysis, design and development of Electronics Systems as well as to interpret and synthesize experimental data leading to valid conclusions.
2. Exhibit the skills gathered to analyze, design, develop software applications and hardware products in the field of embedded systems and allied areas.

Program Educational Objectives (PEOs)

PEO1: Graduates exhibit their innovative ideas and management skills to meet the day to day technical challenges.

PEO2: Graduates utilize their knowledge and skills for the development of optimal solutions to the problems in the field of Electronics and Communication Engineering..

PEO3: Graduates exhibit good interpersonal skills, leadership qualities and adapt themselves for life-long Learning

	VLSI Design and Testing	Semester	6
Course Code	**BEC602**	CIE Marks	50
Teaching Hours/Week (L:T:P: S)	4:0:0:0	SEE Marks	50
Total Hours of Pedagogy	50 Hours	Total Marks	100
Credits	04	Exam Hours	3 Hours
Examination nature (SEE)	Theory		

Course objectives:

1. This course deals with analysis and design of digital CMOS integrated circuits.
2. The course emphasizes on basic theory of digital circuits, design principles and techniques for digital design blocks implemented in CMOS technology.
3. This course will also cover switching characteristics of digital circuits along with delay and power estimation.
4. Understanding the CMOS sequential circuits and memory design concepts.
5. Explore the knowledge of VLSI Design flow and Testing.

Teaching-Learning Process (General Instructions)

These are sample Strategies; that teachers can use to accelerate the attainment of the various course outcomes.

1. Lecture method (L) does not mean only traditional lecture method, but different type of teaching methods may be adopted to develop the outcomes.
2. Show Video/animation films to explain the different concepts of Digital Signal Processing
3. Encourage collaborative (Group) Learning in the class
4. Ask at least three HOTS (Higher order Thinking) questions in the class, which promotes critical thinking
5. Adopt Problem Based Learning (PBL), which fosters students' Analytical skills, develop thinking skills such as the ability to evaluate, generalize, and analyse information rather than simply recall it.
6. Topics will be introduced in a multiple representation.
7. Show the different ways to solve the same problem and encourage the students to come up with their own creative ways to solve them.
8. Discuss how every concept can be applied to the real world - and when that's possible, it helps improve the students' understanding.
9. Adopt Flipped class technique by sharing the materials / Sample Videos prior to the class and have discussions on the that topic in the succeeding classes.

MODULE-1

Introduction to CMOS Circuits: Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison.

[Text 1: 1.1,1.2,1.3,1.4,1.5.1.6.]

Teaching-Learning Process: Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2

MODULE-2

MOS Transistor Theory: n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage, Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin, Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS. [Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.]

MODULE-3

CMOS Process Technology: Silicon Semiconductor Technology, CMOS Technologies, Layout Design Rules. [Text 1: 3.1,3.2,3.3.]

Circuit Characterization and Performance Estimation: Introduction, Resistance Estimation, Capacitance Estimation, Switching Characteristics, CMOS gate transistor sizing, Determination of conductor size, Power consumption, Charge sharing, Scaling of MOS transistor sizing, Yield. [Text 1: 4.1,4.2,4.3,4.4,4.5.4.6.4.7,4.8,4.9,4.10]

Teaching-Learning Process:

Chalk and talk method/Power point presentation, YouTube Videos RBT Level: L1, L2, L3.

MODULE-4

CMOS Circuit and Logic Design: Introduction, CMOS Logic structures, CMOS Complementary logic, Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body effect, Physical Layout of Logic gates, Input output Pads. [Text 1: 5.1,5.2,5.2.1, , 5.2.2, 5.2.3, 5.2.4, 5.2.6, 5.2.8, 5.3,5.3.1,5.3.2, 5.3.4 ,5.3.8,5.5]

Teaching-Learning Process:

Chalk and talk method, YouTube videos, Power point presentation RBT Level: L1, L2, L3.

MODULE-5

Sequential MOS Logic Circuits: Introduction, Behaviour of Bistable Elements (Excluding Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch, Clocked JK Latch.[Text2: 8.1, 8.2, 8.3, 8.4]

Structured Design and Testing: Introduction, Design Styles, Testing[Text1: 6.1, 6.2. 6.5]

Teaching-Learning Process:

Chalk and talk method/Power point presentation RBT Level: L1, L2, L3

Text Books:

1. Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company.
2. "CMOS Digital Integrated Circuits: Analysis and Design", Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.

Reference Books:

1. "CMOS VLSI Design- A Circuits and Systems Perspective", Neil H E Weste, and David Money Harris 4th Edition, Pearson Education.
2. "Basic VLSI Design", Douglas A Pucknell, Kamran Eshraghian, 3rd Edition, Prentice Hall of India publication, 2005

Course Outcomes: After completing the course, the students will be able to	
CO1	Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors
CO2	Design and realize combinational, sequential digital circuits and memory cells in CMOS logic.
CO3	Analyze the synchronous timing metrics for sequential designs and structured design basics.
CO4	Understand designing digital blocks with design constraints such as propagation delay and dynamic power dissipation.
C05	Understand the concepts of Sequential circuits design and VLSI testing

Generations of ICs :-

Year	Generation	No of T	Examples
1961	SSI	10-100	Logic Gates, FF, ~~counters~~
1966	MSI	100-1000	Adders, mux, counters.
1971	LSI	1000-20000	8bit Mps, RAM, ROM
1980	VLSI	20000 - 1 million	16 & 32 bit Mps, DRAM
1990	WLSI	1-10 million	DSPs, Smart Sensors.
2000	GSI	> 10 million	ASICs, SoC

Moore's Law : (Gordon moore, 1965)

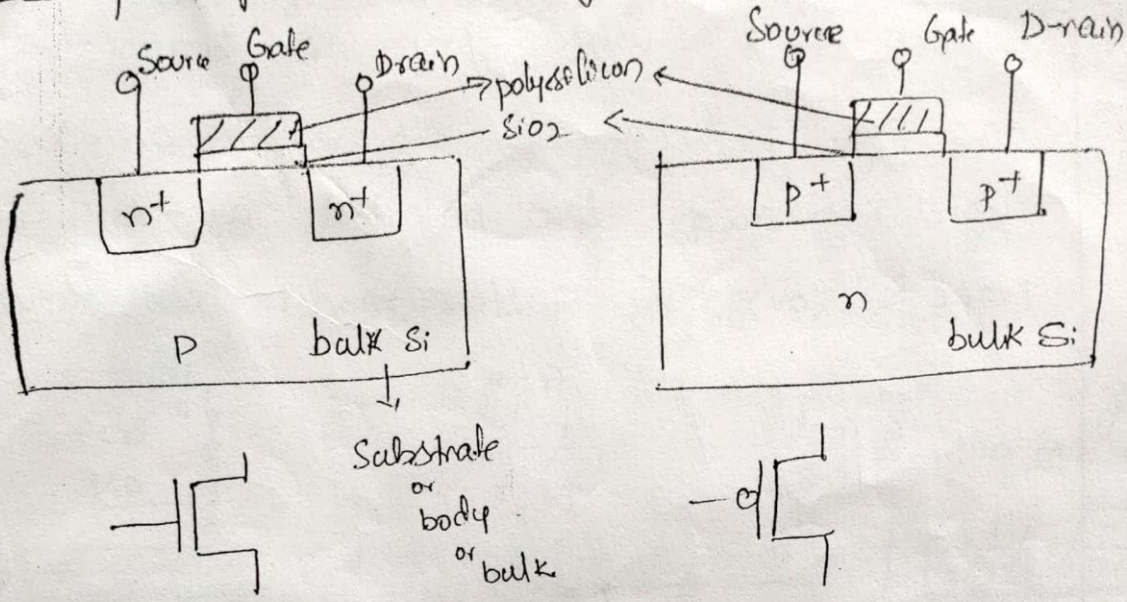
"The number of transistors integrated on IC doubles for every 18 months".

Truly the 1970s, 80s, 90s may be regarded as Integrated circuit era.

MOS Transistors : (metal oxide semiconductor)

MOS structures are created by superimposing several layers of conducting and insulating materials to form a sandwich like structure. CMOS technology provides two types of transistor an n-type and p-type transistor. Transistor operation is based on electric fields hence they are called as field effect transistor

cross section and symbols of these ① & ② are shown. The n^+ and p^+ regions indicate heavily doped n or p type Silicon.



nmos transistor

pmos Transistor

An nmos transistor is built with a p type body and has region of n type semiconductor adjacent to gate called the source and drain. They are physically equivalent and interchangeable. The body is typically grounded.

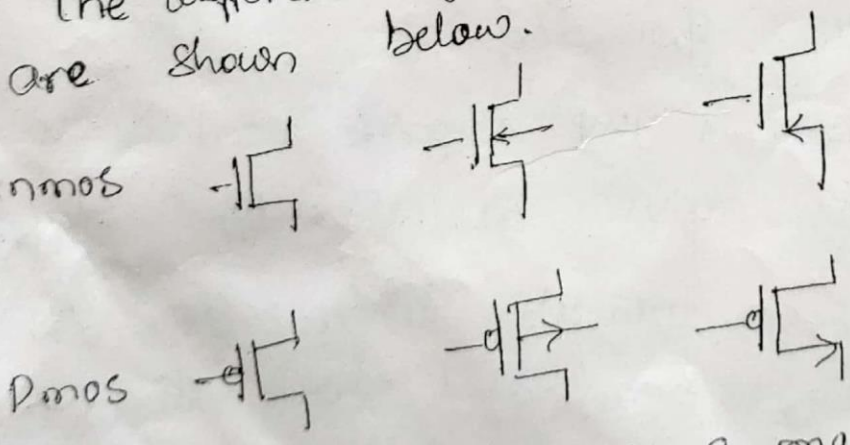
A pmos transistor is just opposite, contains p type source and drain regions with n type body.

For a nmos transistor when g = 0, P-n junctions of the source and drain to body are reverse biased and transistor is OFF. When g = 1 transistor is ON.

For a pmos transistor, when g=0, transistor is ON and when g=1, the transistor is OFF. The high potential is represented as V_{DD} or logic '1' (5v) and low potential as GND or V_{SS} a Logic '0' (0v). The switch model is shown below

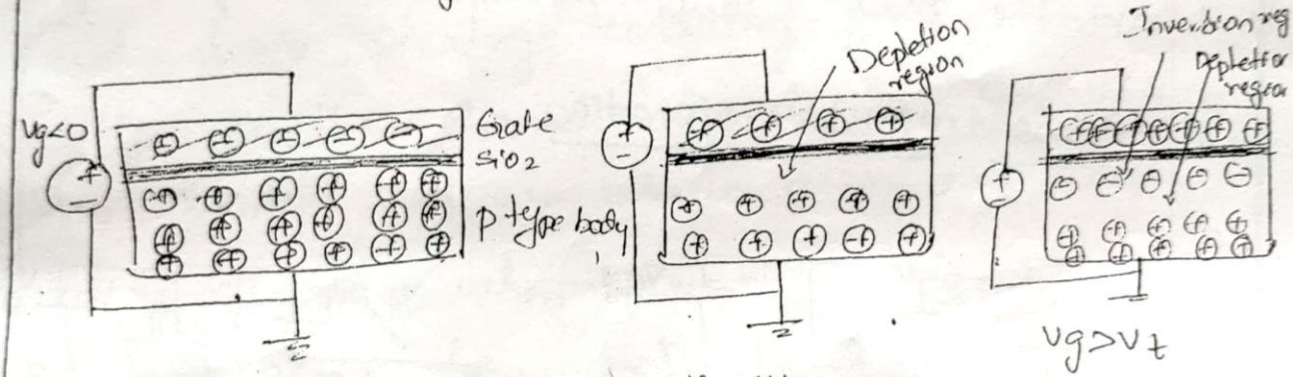
mos Transistor Theory :-

The different Symbols used for mos transistors are shown below.



The mos transistor is a majority carrier device in which the current in a conducting channel between the source and drain is controlled by gate voltage. In nmos electron are majority carriers and in pmos holes are majority carriers.

To study the behavior of mos transistor. Consider a mos structure with gate and body but no source or drain. Fig shows simple mos structure. The top layer is good conductor called as gate made up of polysilicon. The middle layer is thin insulating film of SiO_2 called gate oxide. The bottom layer is the doped Silicon body (p) The body is grounded and voltage is applied to gate



(a) accumulation (b) Depletion (c) Inversion

In fig (a), -ve voltage is applied to the gate, so there is negative charge on the gate. The free holes are attracted by -ve Vg on gate and gets collected under the gate. Thus it called accumulation mode.

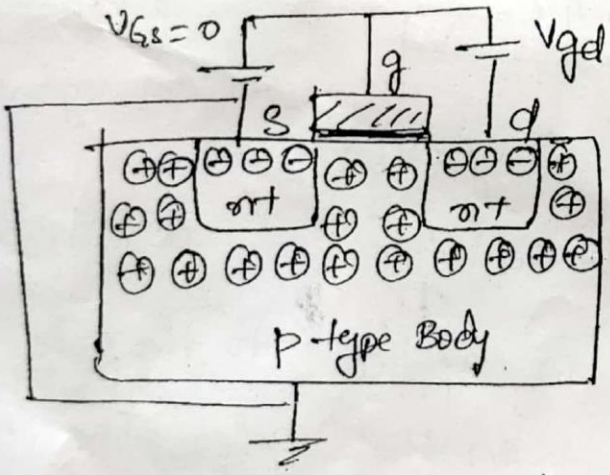
In fig (b) low +ve Vg on gate, repels the holes and resulting in a depletion region forming below the gate

In fig(c) higher +ve potential is applied to gate.

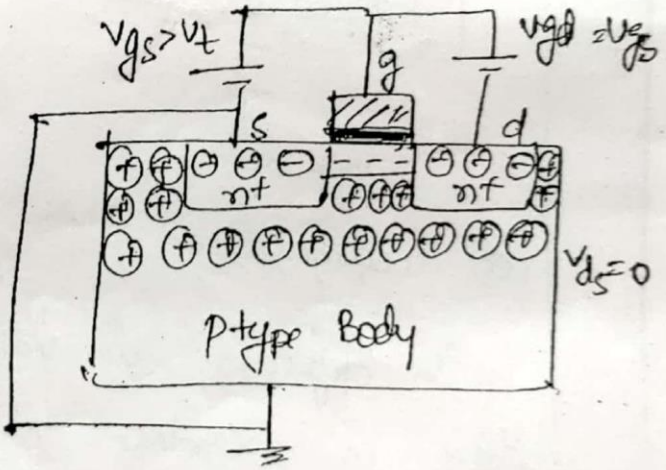
such that $V_g > V_t$. The holes are repelled further and small number of free electrons in the body are attracted to the region beneat the gate. Thin conductive layer of electron in the p-type body is called the 'inversion layer'

The threshold vlg V_t depends on number of dopants in the body and thickness t_{ox} of the oxide.

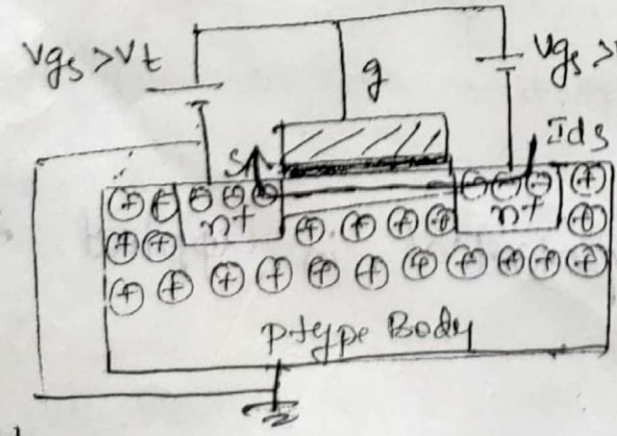
nmos transistor operation :-



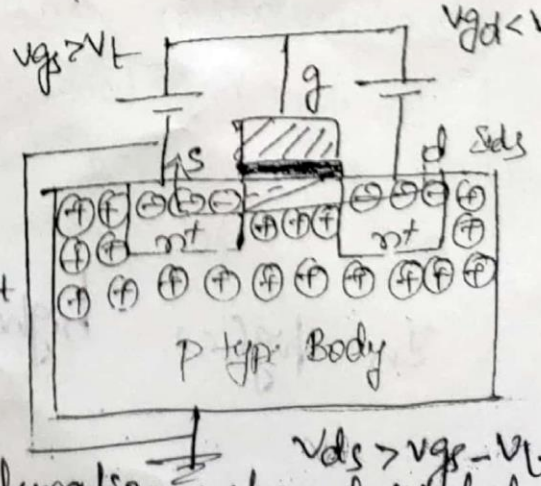
(a) cutoff : No channel
$I_{ds} = 0$



(b) Linear, channel formed
I_{ds} increases with V_{ds}



Linear



$V_{ds} > V_g - V_t$
Saturation : channel pinched off
I_{ds} is independent of V_{DS}

In fig (a), $V_{gs} < V_t$. The source and drain (4) have free electron. The body has free holes but not free electrons. The junction between the body and source or drain are reverse biased so no current flows. This mode of operation is called cutoff.

In fig(b) $V_{gs} > V_t$. Now the inversion region of electron called the channel connects source and drain, creating conducting path. The conductivity in the channel depends on gate voltage. The potential difference between drain and source is $V_{ds} = V_{gs} - V_{gd}$. when $V_{ds} = 0$ ie $V_{gs} = V_{gd}$, no current flows from drain to source.

In fig(c), a small positive potential is applied to drain, therefore current I_{ds} flows through channel from drain to source. This mode of operation is called linear, resistive, non saturated or unsaturated. This current I_{ds} increases with drain vlg and gate vlg

Fig(d), V_{ds} is sufficiently large such that $V_{gd} < V_t$ the channel is no long inverted near the drain and becomes 'pinched off'. Now I_{ds} becomes independent of V_{ds} and controlled by only gate vlg. This mode is called saturation.

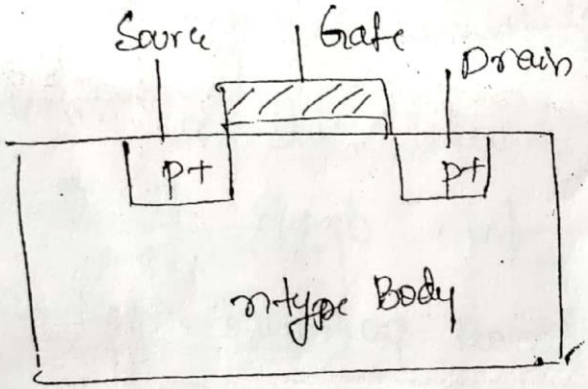
Summary of nmos (1)

$V_{gs} < V_t \rightarrow$ cutoff $\quad I_{ds} = 0$

$V_{gs} > V_t$, V_{ds} small $\rightarrow$ linear region $\rightarrow$ I_{ds} flows.

$V_{gs} > V_t$ & V_{ds} is large $\rightarrow$ acts as current source $\rightarrow$ I_{ds} becomes independent of V_{DS}

The pmos transistor operates in just the opposite way.



Ideal I-V characteristics : (long channel I-V theory)

In linear and saturation region, the gate attracts carriers to form a channel. The carriers drift from source to drain at a rate proportional to electric field b/w S and D. nmos structures looks like 1 pl plate capacitor while operating in inversion.

We can find currents if we know the amount of charge in the channel and rate at which it moves

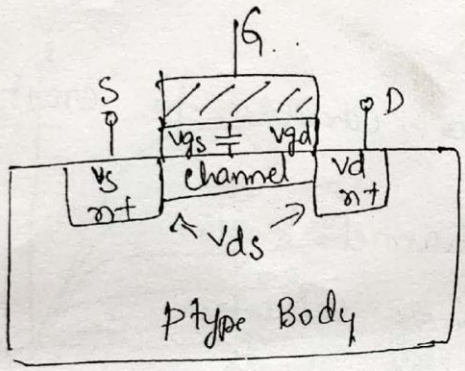
∴ we know that $Q = CV$.

Then the charge in the channel is

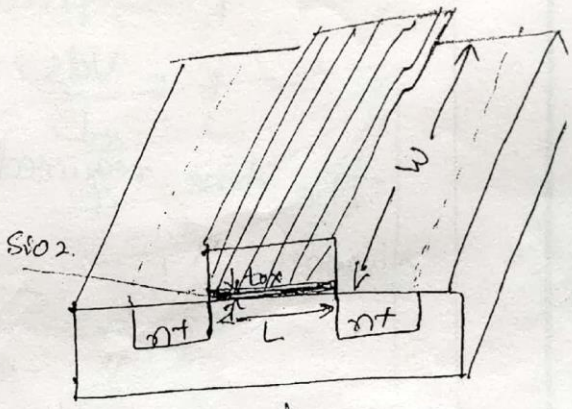
$Q_{channel} = C_g (V_{gc} - V_t)$

where $C_g \rightarrow$ Gate to channel capacitance

$V_{gc} - V_t \rightarrow$ V/g attracting charge to channel to invert from p to n.



Avg Gate to channel potential



Transistor dimension.

If the source is at V_s and drain is at V_D, then the average is $V_c = \frac{(V_s + V_d)}{2}$

$\therefore V_c = V_s + \frac{V_{ds}}{2}$ $\left[\because \frac{2V_s + V_{ds}}{2} = \frac{2V_s + V_d - V_s}{2} = \frac{V_s + V_d}{2}\right]$.

The mean diff b/w gate & channel potential is, $V_{gc} = \frac{(V_{gs} + V_{gd})}{2} = V_{gs} - \frac{V_{ds}}{2}$

If the gate has length L and width W and the oxide thickness is t_{ox} as shown, the capacitance is

$$C_g = \varepsilon_{ox} \frac{WL}{t_{ox}}$$

where $\varepsilon_{ox} = 3.9\varepsilon_0$ for SiO_2 and ε_0 is the permittivity of free space, 8.85×10^{-14} F/cm.

and $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ $\therefore \boxed{C_g = C_{ox} WL}$

Each carrier in the channel is accelerated to velocity

$v = \mu E$

where $\mu \rightarrow$ mobility

$E \rightarrow$ electric field

$E = \frac{V_{ds}}{L}$

The time required for carriers to cross the channel is,

$t = \frac{L}{v}$ $\rightarrow$ channel length

$\rightarrow$ carrier velocity

$$\therefore I_{ds} = \frac{Q_{ch}}{t} = \frac{Q_{ch}}{L/v}$$

$$= v \frac{Q_{ch}}{L} = \frac{\mu E}{L} C_g (V_{gc} - V_t)$$

$$= \frac{\mu E C_{ox}}{L} WL \left(V_{gs} - \frac{V_{ds}}{2} - V_t\right) \quad \because E = \frac{V_{ds}}{L}$$

$$= \mu C_{ox} \frac{W}{L} \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) V_{ds}$$

$$\boxed{I_{ds} = \beta \left(V_{gs} - V_t - \frac{V_{ds}}{2}\right) V_{ds}}$$

where $V_{GT} = V_{gs} - V_t$

(or) $\beta \left(V_{GT} - \frac{V_{ds}}{2}\right) V_{ds}$

where $\beta = \mu C_{ox} \frac{W}{L}$

If $V_{ds} > V_{dsat} = V_{gs} - V_t$, then we get,

$$\boxed{I_{ds} = \frac{\beta}{2} (V_{gs} - V_t)^2}$$

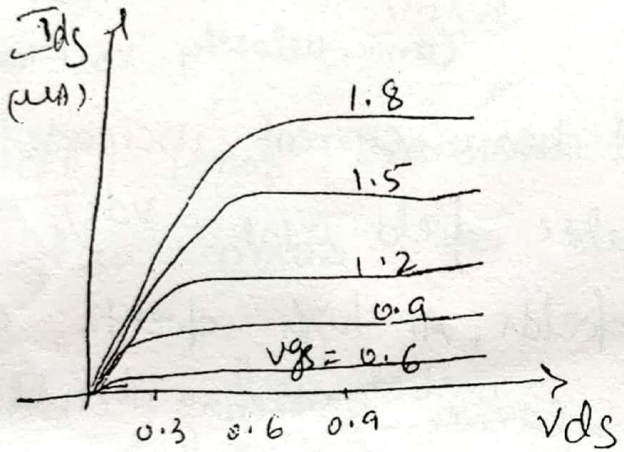
when $(V_{gs} - V_t) = V_{GT}$

$$\boxed{I_{ds} = \beta/2 \, V_{GT}^2}$$

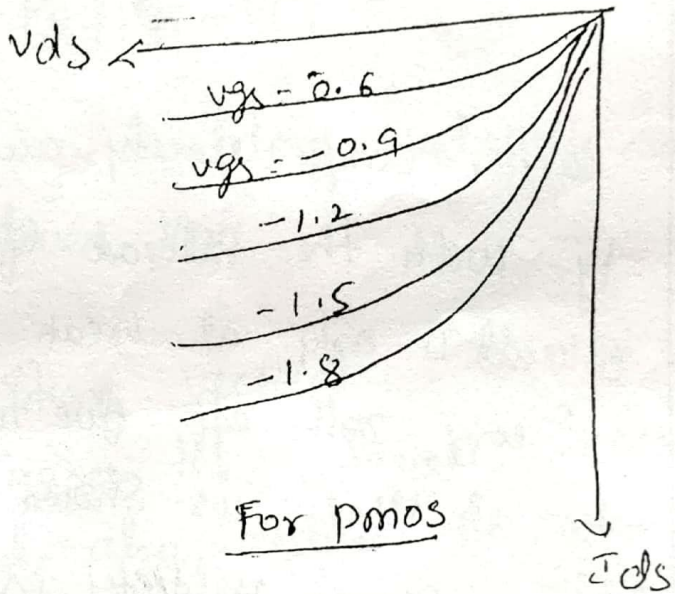
Summary

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{Saturation} \end{cases}$$

Fig below shows IV char of transistor



For nmos

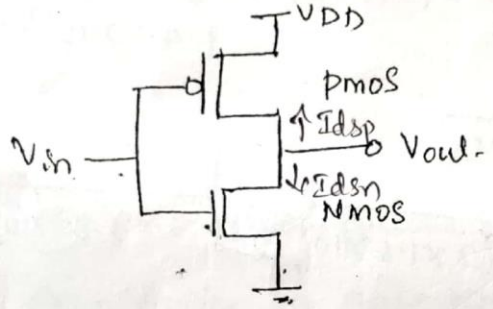


For pmos

** DC Transfer characteristics :-

The DC transfer characteristics relate the output Vtg to the input voltage, assuming that input voltage changes slowly so that internal capacitance can charge or discharge fully.

Consider a complementary CMOS inverter as shown



DC transfer function is plot b/w Vout and Vin

Relations between voltages for the 3 region of operation

	cutoff	linear	Saturation
nmos	$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} \leq V_{gsn} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gsn} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$
pmos	$V_{gsp} \geq V_{tp}$ $V_{in} \geq V_{tp} + V_{DD}$	$V_{gsp} \leq V_{tp}$ $V_{in} < V_{tp} + V_{DD}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{DD}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$

V_{tn} → Threshold voltage for nmos

V_{tp} → Threshold voltage for pmos

V_{tp} is negative.

As the Source of nmos transistor is grounded, $V_{gsn} = V_{in}$ and $V_{dsn} = V_{out}$.

As the Source of pmos transistor is connected to V_{DD}, $V_{gsp} = V_{in} - V_{DD}$ and $V_{dsp} = V_{out} - V_{DD}$.

To find the tranfer char (Vout vs Vin), assume,

$$I_{dsn} = |I_{dsp}|$$

$$V_{tp} = -V_{tn}$$

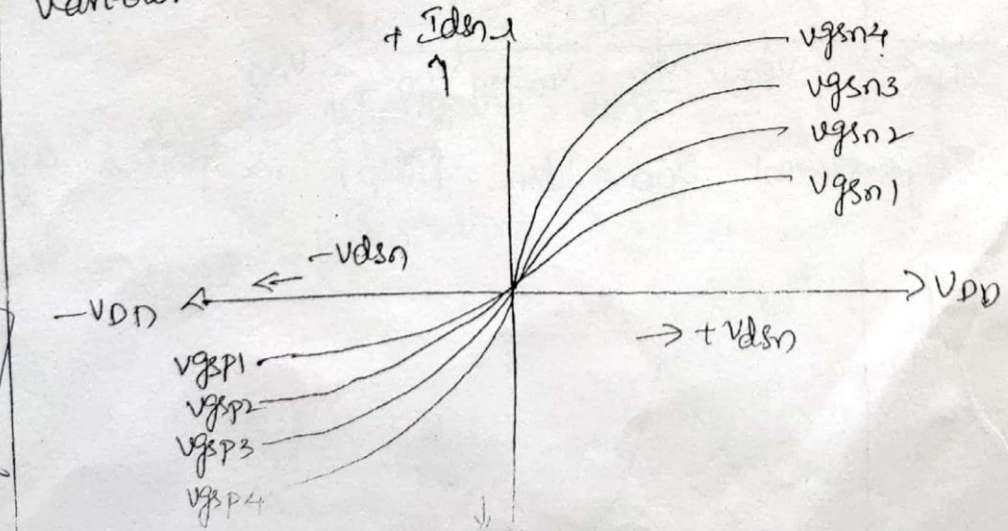
$$\beta_n = \beta_p$$

The important equation for mos transistors are

$$I_{DS} = \beta\left(V_{gs} - V_t - \frac{V_{DS}}{2}\right) V_{DS}$$

& $$I_{DS} = \frac{\beta}{2}(V_{GS} - V_t)^2$$

A plot of I_{dsn} and I_{dsp} interms of V_{dsn} & V_{dsp} for various values of V_{gsn} and V_{gsp} is shown.



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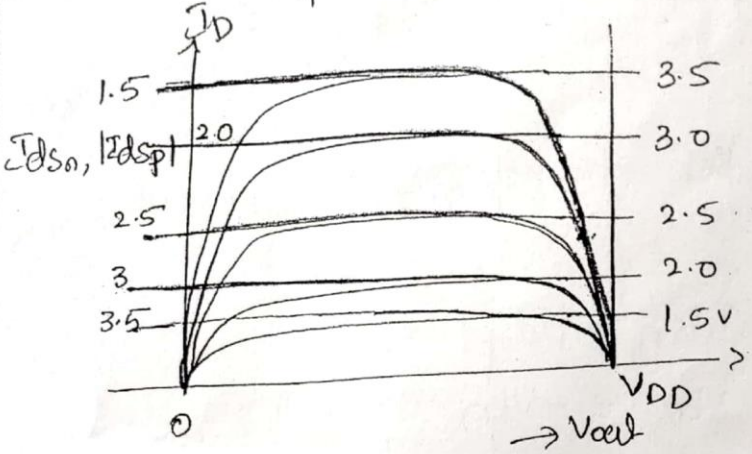
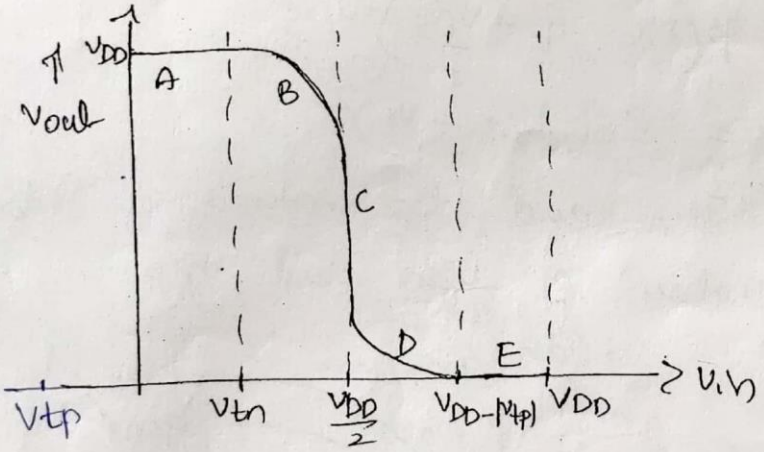
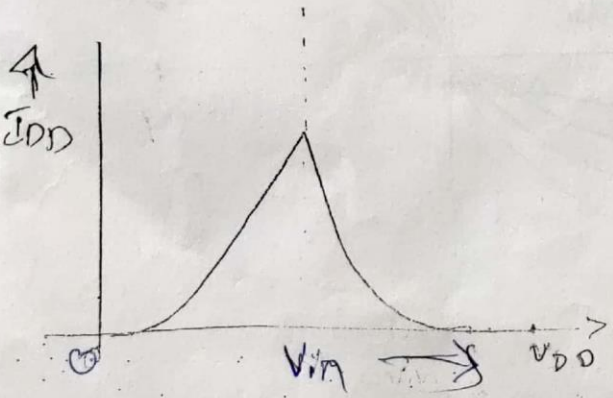
The same plot of I_{dsn} and $|I_{dsp}|$ in terms of V_{out} for various values of V_{in} is shown.



The inverter transfer chars V_{out} vs V_{in} is shown



The supply current $I_{DD} = I_{dsn} = |I_{dsp}|$ is plotted against V_{in}.

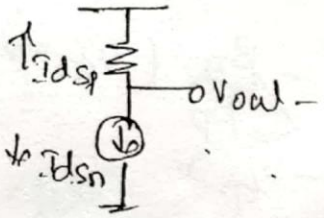


Region A. The region is defined by $0 \le V_{in} \le V_{tn}$ where Nmos - cutoff and pmos - linear.

The o/p v/g is $V_{out} = V_{DD}$

Region B. This region is defined by $V_{tn} \le V_{in} < \frac{V_{DD}}{2}$ where pmos - linear ($V_{ds} \neq 0$), Nmos - Satn region

The equivalent ckt is given by,



I_{dsn} is obtained by $V_{gs} = V_{in}$

For N Device
$V_{gs} = V_{in}$
$V_{DS} = V_{out}$

$$I_{dsn} = \beta_n \frac{[V_{in} - V_{tn}]^2}{2}$$

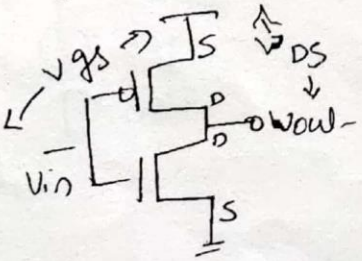
where $\beta_n = \mu_n \frac{\epsilon_{ox}}{t_{ox}} \left[\frac{W_n}{L_n}\right]$

Current in p device is given by,

W.K.T, $V_{gs} = V_{in} - V_{DD}$

$V_{ds} = V_{out} - V_{DD}$

$$\therefore I_{DSP} = \beta\left[(V_g - V_t) V_{ds} - \frac{V_{DS}^2}{2}\right]$$



$$I_{DSP} = \beta\left[(V_{in} - V_{DD} - V_{tp})(V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2}\right]$$

where $\beta_p = \mu_p \frac{\epsilon_{ox}}{t_{ox}} \left[\frac{W_p}{L_p}\right]$

KVL

$$I_{dsp} = -I_{dsn}$$

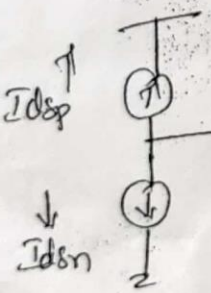
$$\beta_p (V_{in} - V_{DD} - V_{tp})(V_{out} - V_{DD}) - \frac{(V_{out} - V_{DD})^2}{2} = \beta_n \frac{[V_{in} - V_{tn}]^2}{2}$$

Solving we get-

$$V_{out} = (V_{in} - V_{tp}) + (V_{in} - V_{tp})^2 - \frac{\beta_n}{\beta_p}(V_{in} - V_{tn})^2 - 2V_{DD}\left(V_{in} - \frac{V_{DD}}{2} - V_{tp}\right)$$

$$V_{out} = (V_{in} - V_{tp}) + \sqrt{(V_{in} - V_{tp})^2 - \frac{\beta_n}{\beta_p}(V_{in} - V_{tp})^2 - 2\left(V_{in} - \frac{V_{DD}}{2} - V_{tp}\right)V_{DD}}$$

Region C: Here both n and p transistors are in Saturation as shown in fig below.



$$I_{dsp} = -\frac{\beta_p}{2}(V_{gsp} - V_{tp})^2$$

$$= -\frac{\beta_p}{2}(V_{in} - V_{DD} - V_{tp})^2$$

$$I_{dsn} = \frac{\beta_n}{2}(V_{in} - V_{tn})^2$$

KVL $I_{dsp} = -I_{dsn}$

On substituting and simplifying, we get-

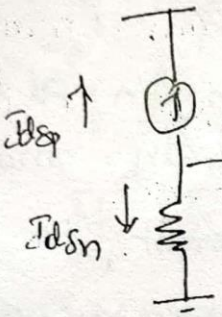
$$V_{in} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

If $\beta_n = \beta_p$ and $V_{tn} = -V_{tp}$, we have

$V_{in} = \frac{V_{DD}}{2}$ and V_{out} drops

Region D :- Here $V_{in} > V_{DD}/2$ and $V_{in} < V_{DD} + V_{tp}$

p device is in Satn and n device is in linear region as shown



$$I_{dsp} = -\frac{\beta_p}{2}(V_{in} - V_{DD} - V_{tp})^2$$

$$I_{dsn} = \beta_n\left[(V_{in} - V_{tn})V_{out} - \frac{V_{out}^2}{2}\right]$$

$$I_{dsn} = -I_{dsp}$$

∴ wkt

$$V_{out} = (V_{in} - V_{tn}) - \sqrt{(V_{in} - V_{tn})^2 - \frac{\beta_p}{\beta_n}(V_{in} - V_{DD} - V_{tp})^2}$$

Region E :- Here $V_{in} > V_{DD} + V_{tp}$.

p device is in cutoff and n device is in linear region

$\therefore V_{out} = 0$

Summary of CMOS inverter operation :-

Region	condition	P Device	N Device	output
A	$0 \le V_{in} \le V_{tn}$	Linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < \frac{V_{DD}}{2}$	Linear	Saturated	$V_{out} > \frac{V_{DD}}{2}$
C	$V_{in} = \frac{V_{DD}}{2}$	Saturated	saturated	V_{out} drops
D	$\frac{V_{DD}}{2} < V_{in} < \frac{V_{DD}}{2} - \lvert V_{tp}\rvert$	Saturated	Linear	$V_{out} < \frac{V_{DD}}{2}$
E	$V_{in} > V_{DD} - \lvert V_{tp}\rvert$	cutoff	Linear	$V_{out} = 0$

Beta Ratio Effects :-

Inverters with different beta ratios β_p/β_n are called skewed inverters.

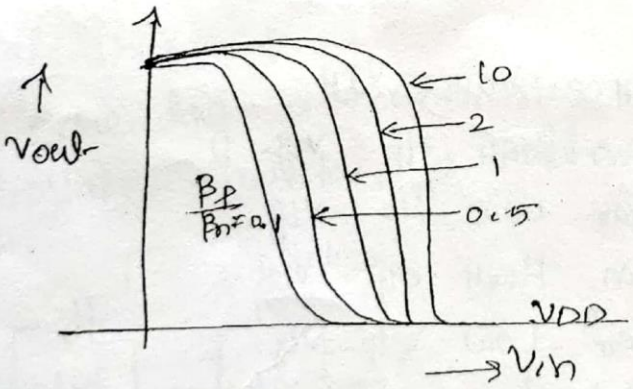
If $\beta_p/\beta_n > 1$, the inverter is HI - skewed.

If $\frac{\beta_p}{\beta_n} < 1$, the inverters is LO - skewed

If $\frac{\beta_p}{\beta_n} = 1$, the inverter is normal or unskewed

High skew inverters has stronger pmos transistor and require higher threshold. LO-skew inverters has weak pmos and thus low switching threshold.

Fig below shows skewing impact on DC transfer char. As beta ratio is changed, the switching threshold moves but the output v/g transition remains sharp.



NOTE: when temp is raised, mobility (μ) decreases
$\therefore$ β_p/β_n ratio decreases, and curves shifts to left.

* Noise Margin :- Noise margin or noise immunity is allowable input gate voltage so that output will not be corrupted. Two parameters are used to specify noise margin, Low noise margin NM_L and HIGH noise margin NM_H.

NM_L is defined as the difference in maximum Low input voltage recognized by the receiving gate and the maximum LOW output voltage produced by the driving gate.

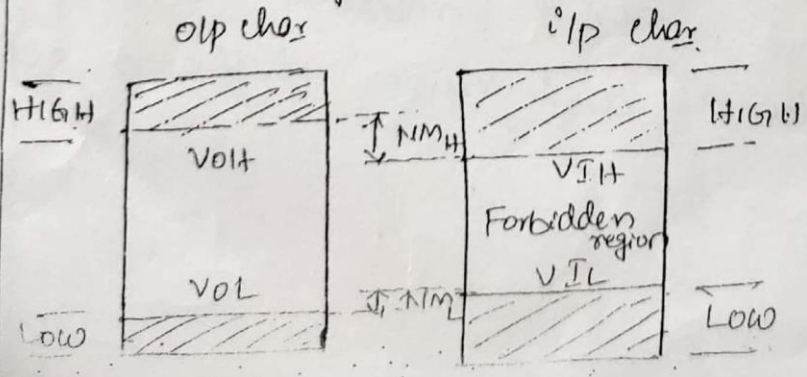
$$NM_L = V_{IL} - V_{OL}$$

NM_H is defined as the difference between the minimum HIGH o/p voltage of driving gate and the minimum HIGH input voltage recognized by the receiving gate. Thus,

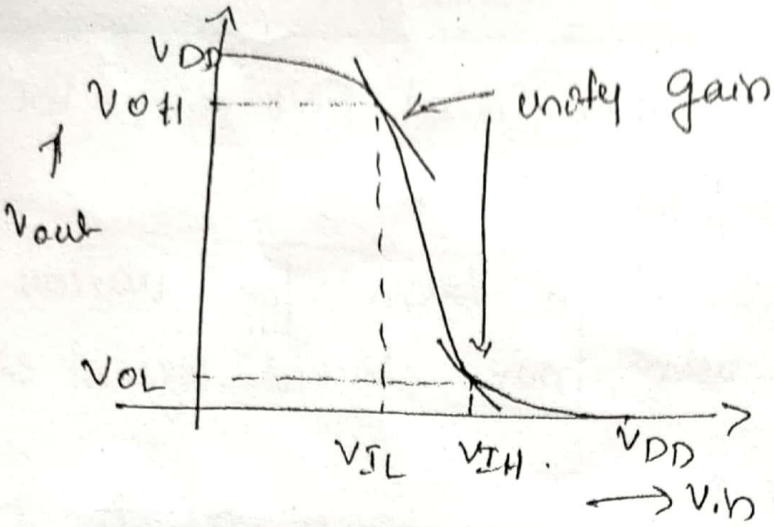
$$NM_H = V_{OH} - V_{IH}$$

where V_{IH} → min HIGH i/p voltage
V_{IL} → max LOW i/p voltage
V_{OH} → min HIGH o/p voltage
V_{OL} → max LOW o/p voltage.

Noise margin definitions are shown below.



The voltage levels on transfer char are shown in fig (3)



It is desirable to have V_{IH} and V_{IL} should be close to each other ie to switch transfer char$_n$ abruptly.

Typical values of noise margin are

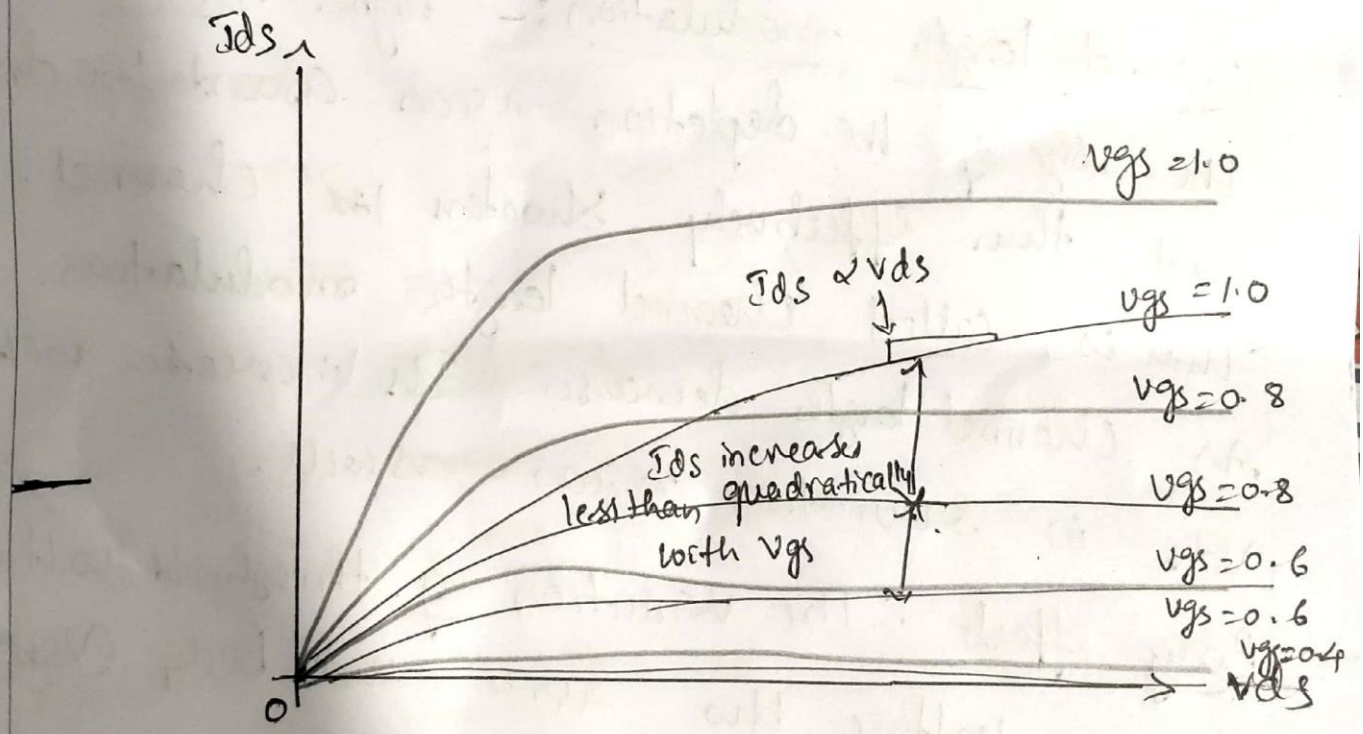
$$NM_L = 0.46\, V_{DD}$$
$$NM_H = 0.34\, V_{DD}$$

when input is at worst legal value, the o/p is slightly degraded, called as noise feed through or propagated noise.

Non Ideal IV effects :-

The long channel IV model neglects many effects that are important to devices with channel lengths below 1 micron.

Fig below shows ideal IV characteristics and simulated IV characteristics of a 1u wide nmos transistor in 65 nm process.



The saturation current increases less than quadratically with increasing Vgs. This is due to two effects: velocity saturation & mobility degradation.

Velocity Saturation: At high lateral field strengths (V_{ds}/L), carrier velocity ceases to increase linearly with field strength. This is called

velocity saturation and results in lower I_{ds} than expected at high V_{ds}.

mobility degradation: At high vertical field strengths (V_{gs}/t_{ox}), the carriers scatter off the oxide interface more often, slowing their progress. This results in less current (I_{ds}) than expected at high V_{gs}.

Channel length modulation:- Higher V_{DS} increases the size of the depletion region around the drain and thus effectively shortens the channel. This is called channel length modulation. As channel length decreases I_{ds} increases with V_{ds} in saturation region as well.

Body effect: The variation of threshold voltage due to voltage b/w source and body (V_{sb}) is called body effect.

Subthreshold effect conduction: For $V_{gs} < V_t$, the current drops off exponentially rather than abruptly becoming zero. This is called sub threshold conduction.

Junction leakage: The reverse biased diodes across ~~for~~ conduct small amount of current I_D called as leakage.

$$i_D = i_S \left[e^{V_D/N_T} - 1 \right]$$

Tunnelling :- The current into gate is ideally 0. However as the thickness of gate oxide reduces to only small number of atomic layers, electron tunnel through the gate, causing some gate current. It is called tunneling.

Temp. dependance :- Transistor characteristics are influenced by temp. Carrier mobility decreases with temp. The relation is given by,

$$\mu(T) = \mu(T_r) \left(\frac{T}{T_r} \right)^{-k_\mu}$$

T - absolute temp

T_r - room temp

k_μ - fitting parameter (1.2 - 2.0)

Mobility Degradation and Velocity Saturation:-

The long channel model assumed that carrier mobility is independent of applied field. This assumption is good for low fields but not for stronger fields. The carriers attain maximum velocity v_{sat} when high fields are applied. This is called velocity saturation.

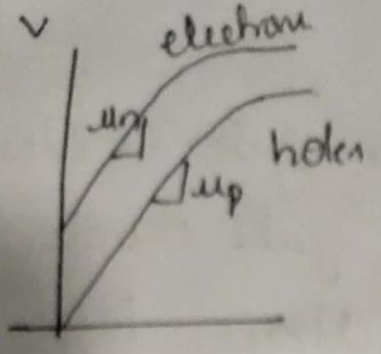


Fig shows carrier velocity v/s electric field E b/w D & S. At low fields, velocity increases linearly with field. The slope is μ_{eff}. At fields above a critical level E_c, the velocity levels out at V_{sat}.

i.e $$v = \begin{cases} \dfrac{\mu_{eff} E}{1 + \dfrac{E}{E_c}} & E < E_c \\ V_{sat} & E \geq E_c \end{cases}$$

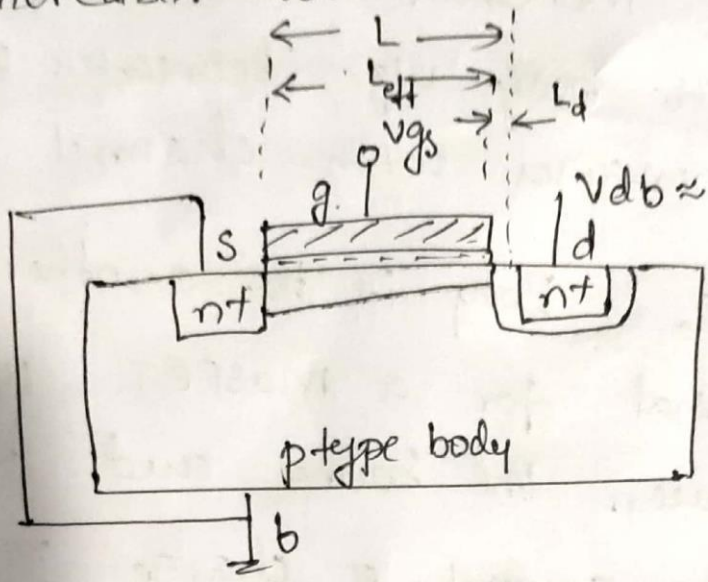
where $$E_c = \frac{2 V_{sat}}{\mu_{eff}}$$

NOTE [Velocity Saturation refers to the limiting of carrier velocity at high field.]

Problem: Find the critical V_g to fully ON nmos and pmos transistors using the effective mobilities

Channel length Modulation :-

As Vds increases, depletion region around drain region increases with a width L_d as shown.



The depletion region effectively shortens the channel length to

$$L_{eff} = L - L_d$$

As Vds increases, channel length decreases and results in higher current., thus Ids increases with Vds in saturation.

$$I_{ds} = \frac{\beta}{2}(V_G - V_t)^2 \left[1 + \frac{V_{ds}}{V_A}\right]$$

where V_A → Early voltage.

V_A is proportional to channel length.

Threshold Voltage Effects :-

So far, we have treated threshold V_{tg} as a constant. However V_t increases with the source V_{tg}, decreases with body V_{tg}, decreases with drain V_{tg} and increases with channel length.

① **Body Effect** :- Body is the another implicit fourth terminal for a MOSFET. When V_{sb} is applied between the source and body, it increases the amount of charge required to invert the channel, hence it increases the V_t. The threshold V_{tg} can be modeled as,

$$V_t = V_{to} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

where V_{to} → threshold V_{tg} when s is at body potential

ϕ_s → Surface potential at threshold

γ → body effect coefficient (0.4 to $1\ V^{1/2}$)

$$\phi_s = 2V_T \ln\frac{N_A}{n_i}$$

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2q\varepsilon_{si}N_A} = \frac{\sqrt{2q\varepsilon_{si}N_A}}{C_{ox}}$$

④ Drain induced Barrier Lowering :-

The drain V/g Vds creates an electric field that affects the threshold V/g. This drain induced barrier lowering (DIBL) effect is important in short channel transistors. It can be modelled as

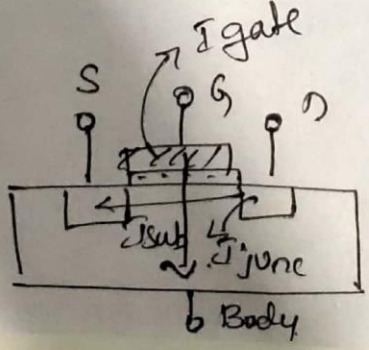
$$V_t = V_{to} - \eta V_{ds}$$

where η is the DIBL coefficient

DIBL also causes Ids to increase with Vds in sat^n.

⑤ Short channel Effect :- The threshold voltage typically increases with channel length. This phenomenon is important for small L where S and D depletion region extend into channel region.

Leakage :- When the transistors are normally OFF, they leak small amounts of current. Different types of leakage currents include subthreshold conduction b/w S and D, gate leakage from G to body and junction leakage from S to body and drain to body, as shown.



Leakage current paths

Subthreshold conduction is caused by thermal emission of carriers over the potential barrier set by the threshold.

Gate leakage is quantum mechanical effect caused by tunneling through the extremely thin gate dielectric.

Junction leakage: is caused by current through the pn jn blw the S/D diffusions and the body