# VLSI DESIGN AND TESTING (BEC602)

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# Module 2 Syllabus

- **MOS Transistor Theory:** n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage,
- Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS
- inverter DC characteristics, Influence of $\beta n$ / $\beta p$ ratio on transfer characteristics, Noise margin,
- Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.
- [Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.]

# MOS symbols

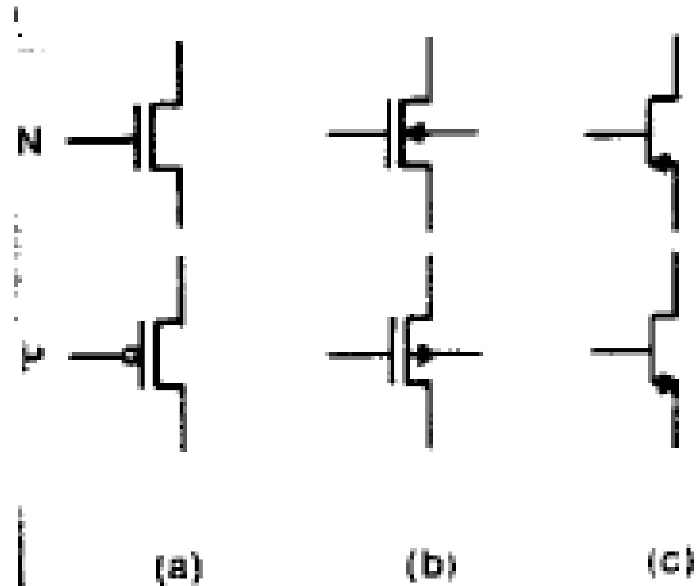
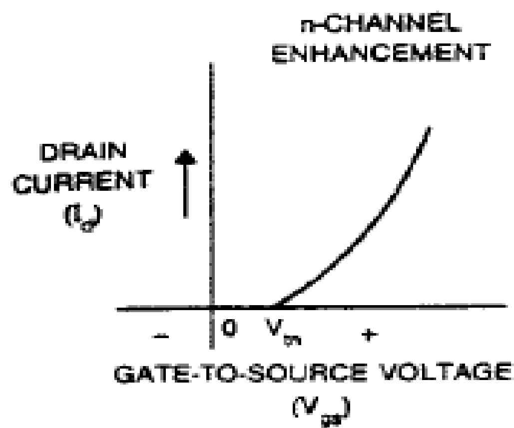
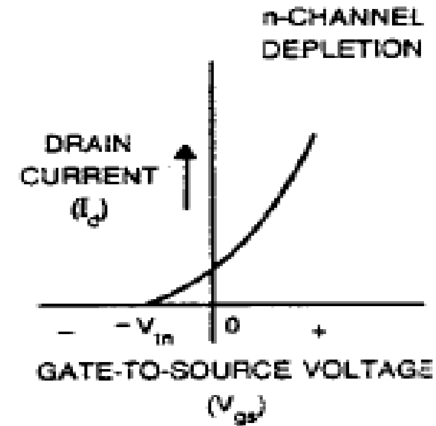
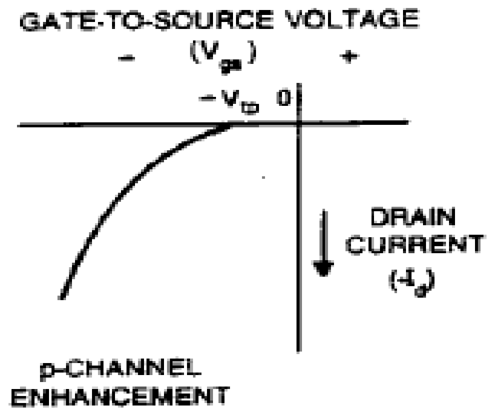


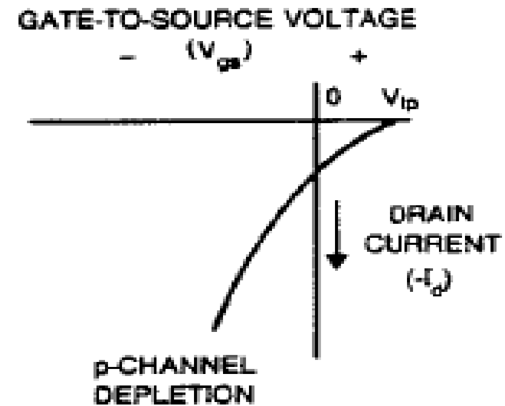

**FIGURE 2.1.** MOS transistor symbols

# Characteristics of MOS

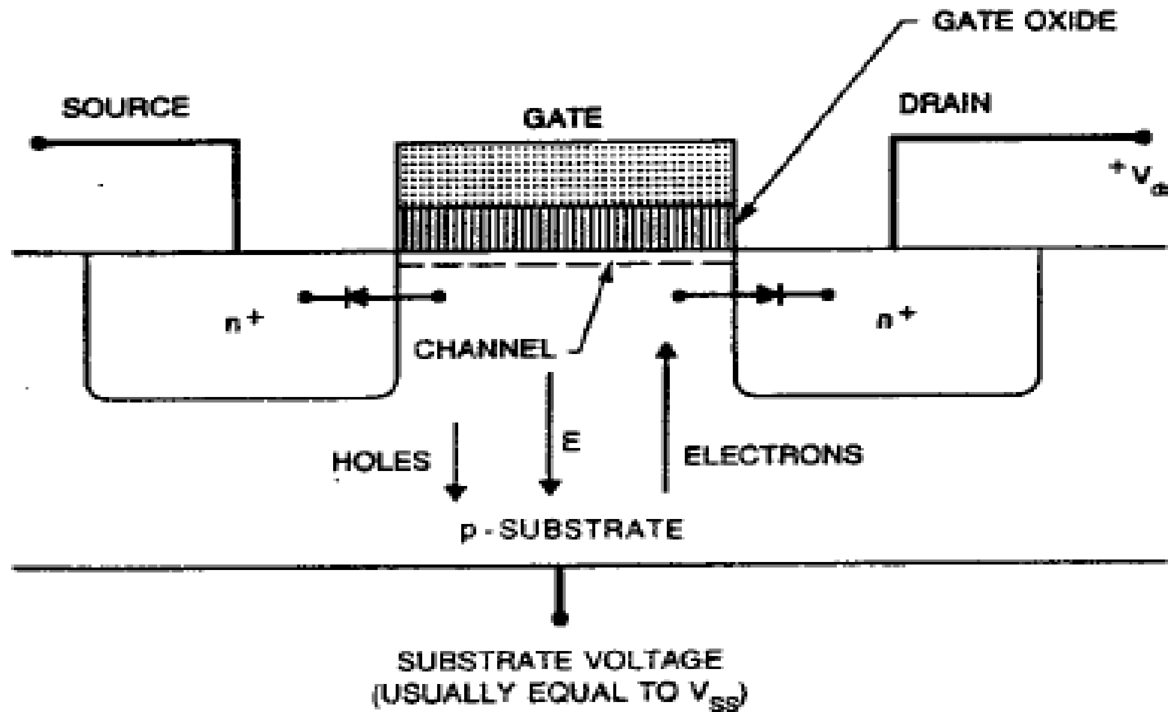


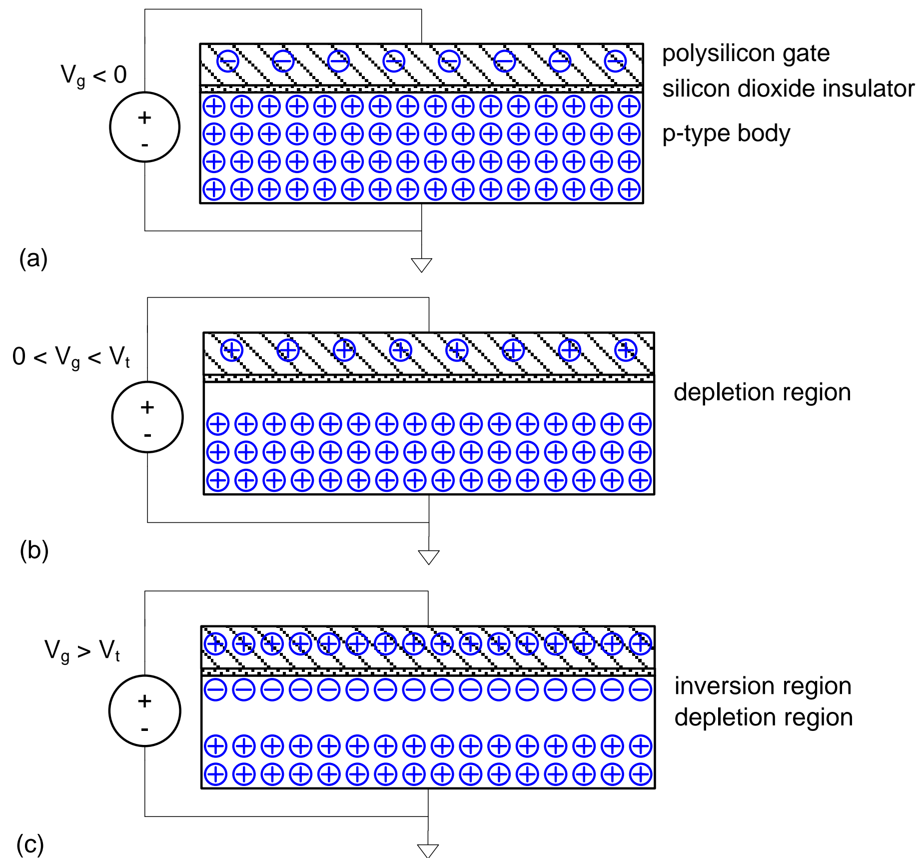



# Structure of NMOS



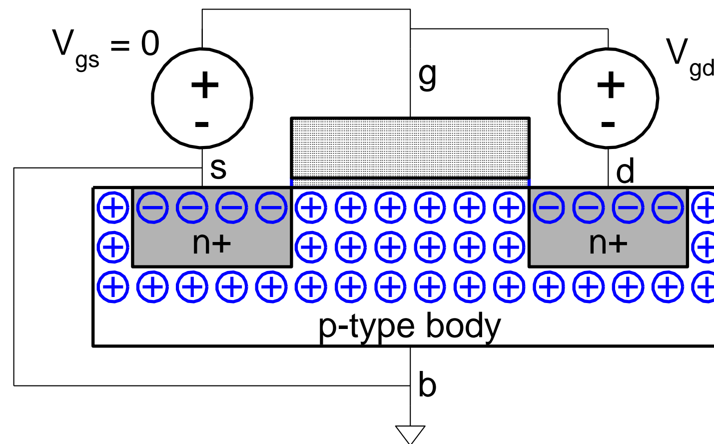
# MOS Capacitor

- Gate and body form MOS capacitor
- Operating modes
  - Accumulation
  - Depletion
  - Inversion



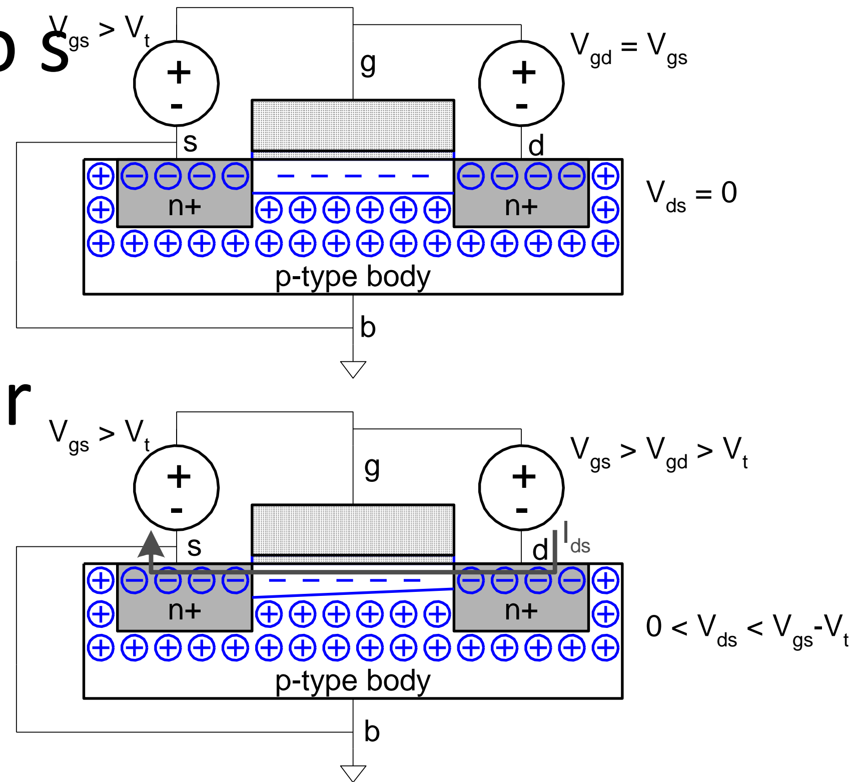
# nMOS Cutoff

- No channel
- $I_{ds} \approx 0$



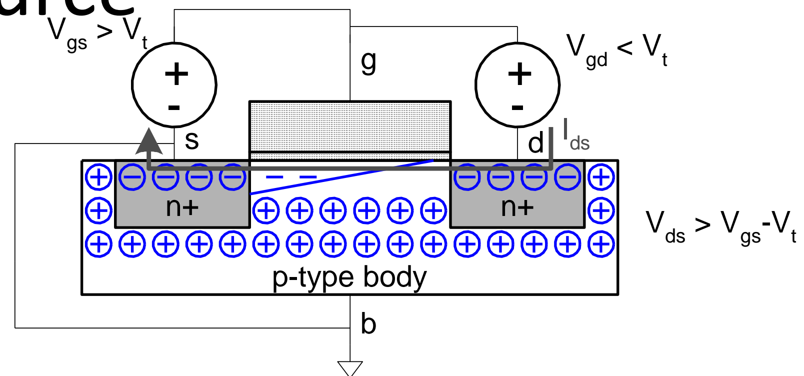
# nMOS Linear

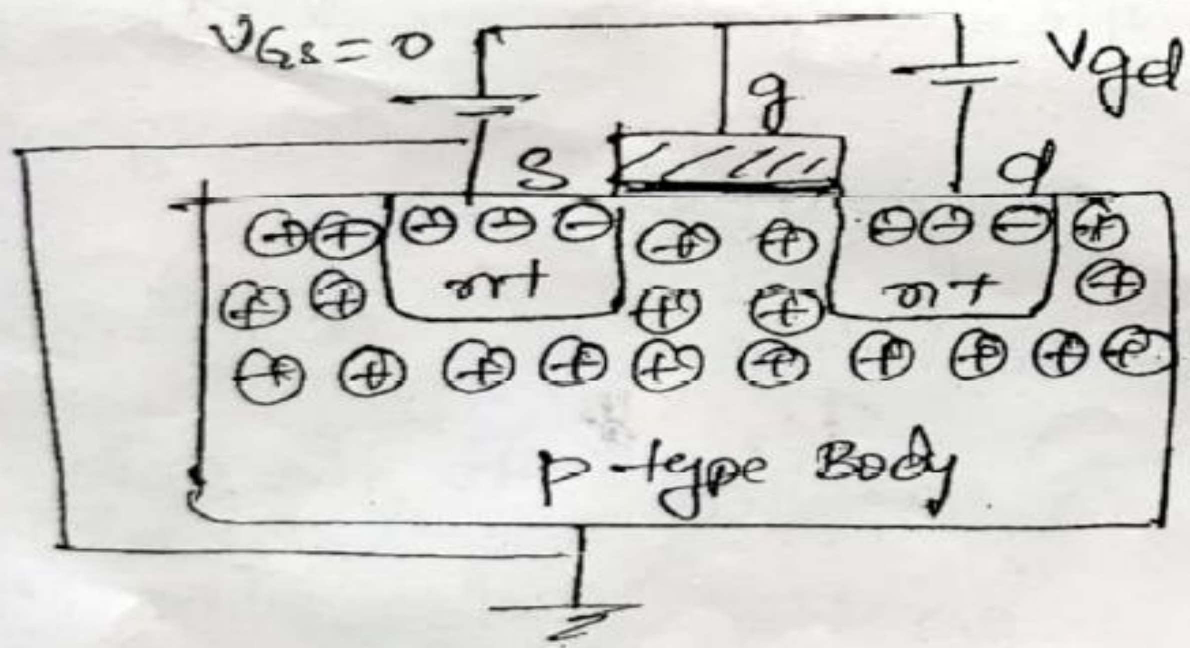
- Channel forms
- Current flows from d to s
  - $e^-$ from s to d
- $I_{ds}$ increases with $V_{ds}$
- Similar to linear resistor



# nMOS Saturation

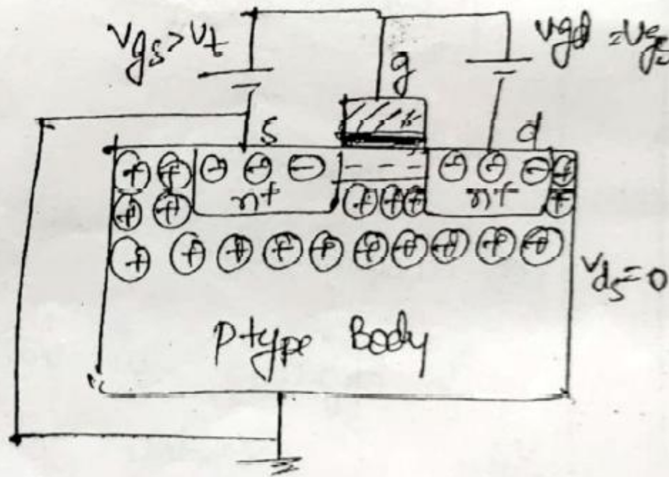
- Channel pinches off
- $I_{ds}$ independent of $V_{ds}$
- We say current *saturates*
- Similar to current source



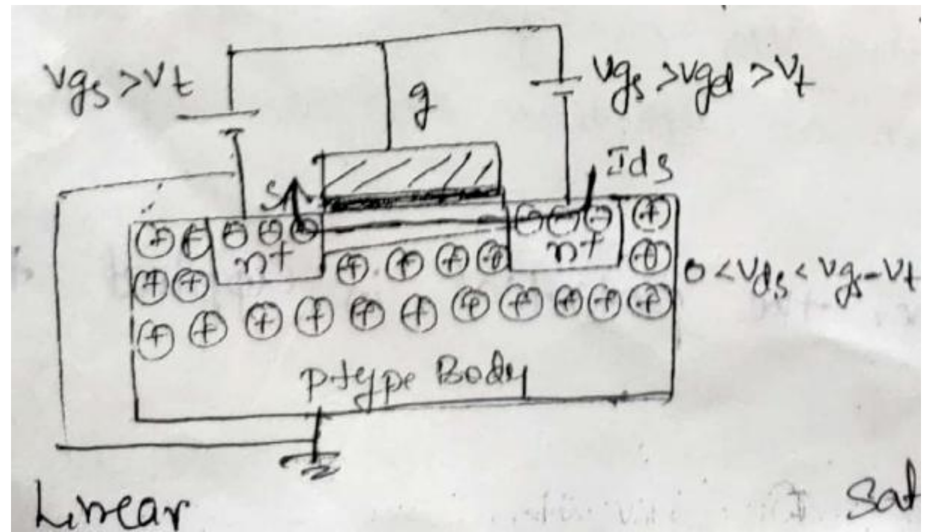



ⓐ cutoff : No channel

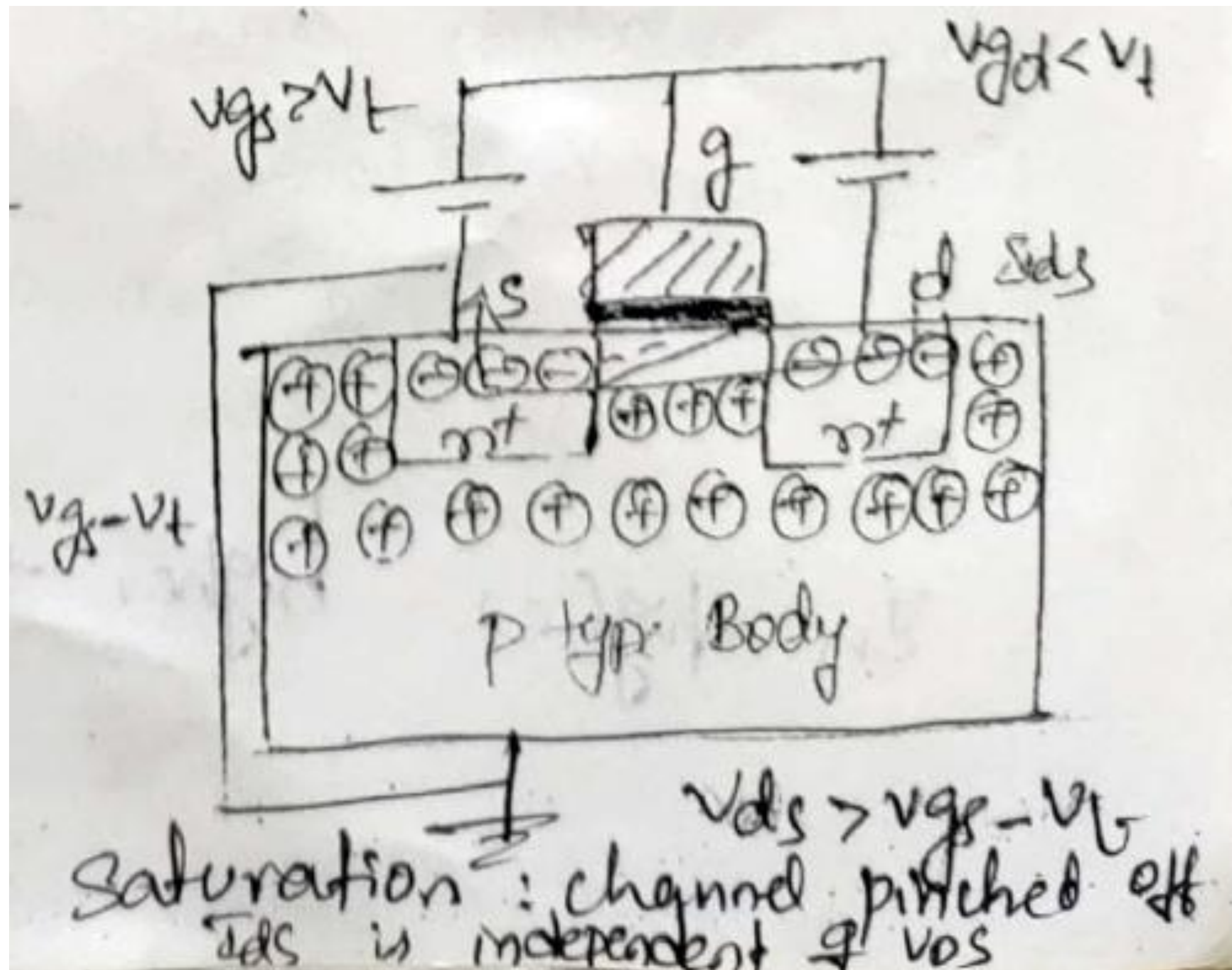
$I_{ds} = 0$



Vgs > Vt
g
s
d
n+
n+
Vds = 0
p-type Body
(b) Linear, channel formed

Vgs > Vt
g
Vgs > Vgd > Vt
Ids
s
n+
n+
0 < Vds < Vgs - Vt
p-type Body
Linear
Sat



vgs > vt
vgd < vt
g
s
d
Ids
n+
n+
vgs - vt
P type Body
Vds > vgs - vt
Saturation : channel pinched off
Ids is independent of Vds

# Summary of NMOS

Summary of nmos ①

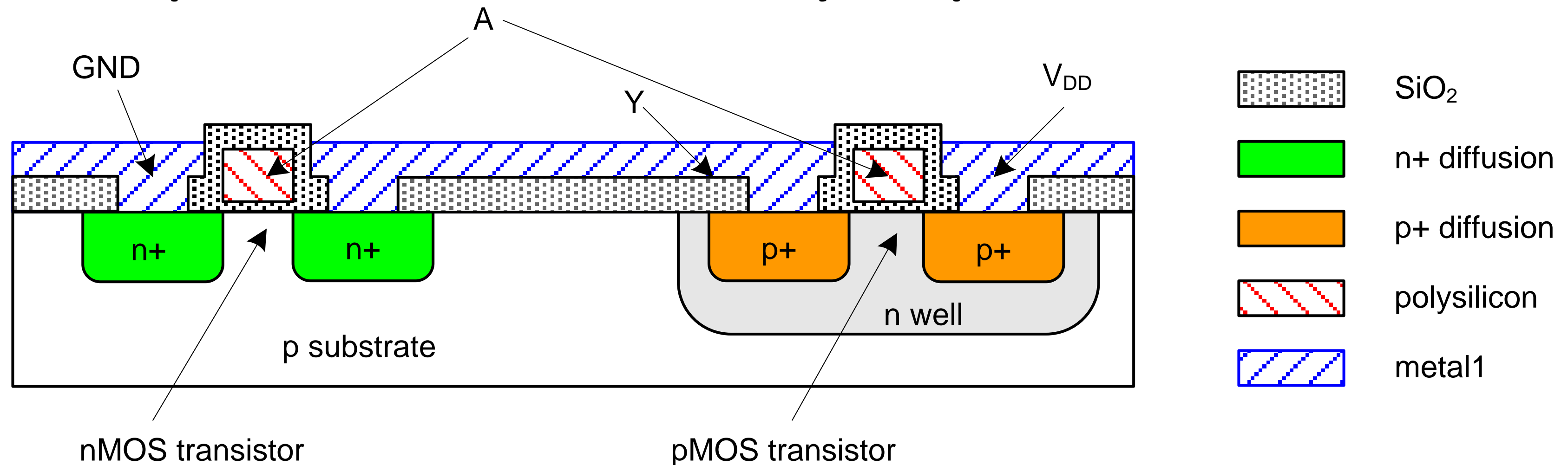
$V_{gs} < V_t$ → cutoff $I_{ds} = 0$

$V_{gs} > V_t$, $V_{ds}$ small → linear region → $I_{ds}$ flows.

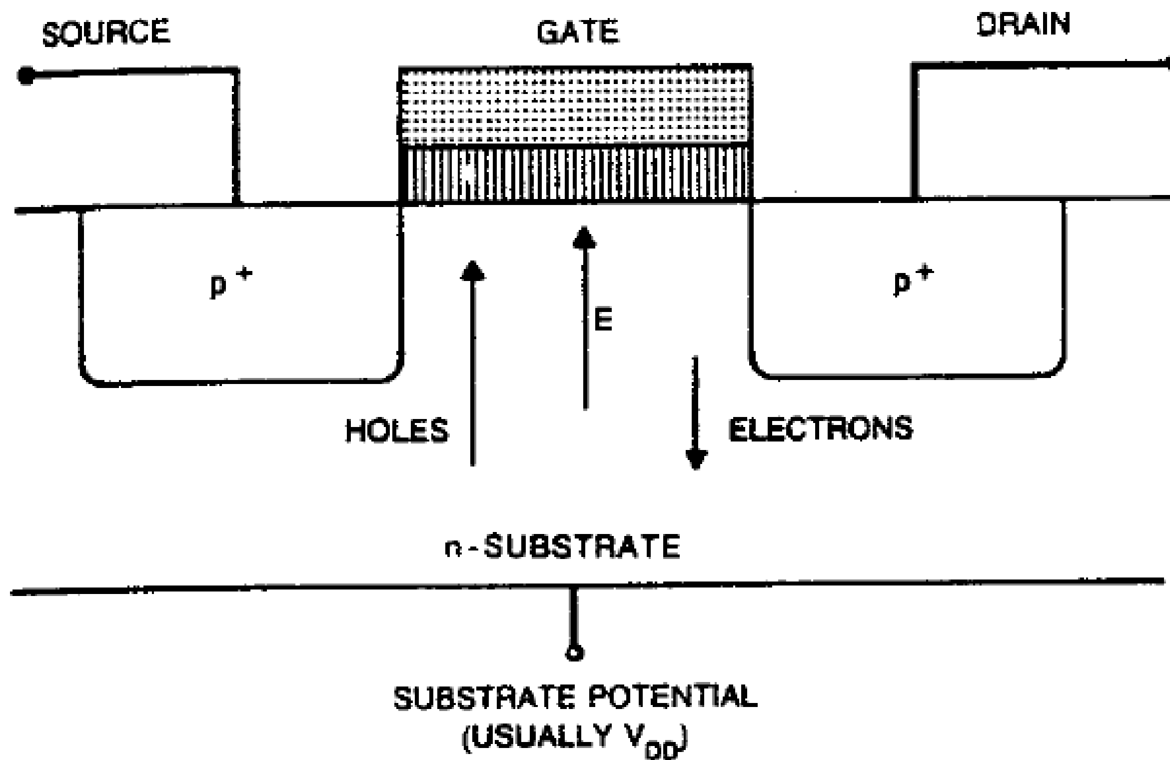
$V_{gs} > V_t$ & $V_{ds}$ is large → acts as current source → $I_{ds}$ becomes independent of $V_{DS}$

# Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors



# PMOS transistor



# Threshlod Voltage

The threshold voltage, $V_t$, for an MOS transistor can be defined as the voltage applied between the gate and source of an MOS device below which the drain-to-source current $I_{ds}$ drops to zero. In general, the threshold voltage is a function of a number of parameters including the following:

- gate material
- gate insulation material
- gate insulator thickness
- channel doping
- impurities at silicon-insulator interface
- voltage between source and substrate $V_{sb}$.

# Threshold voltage adjustment

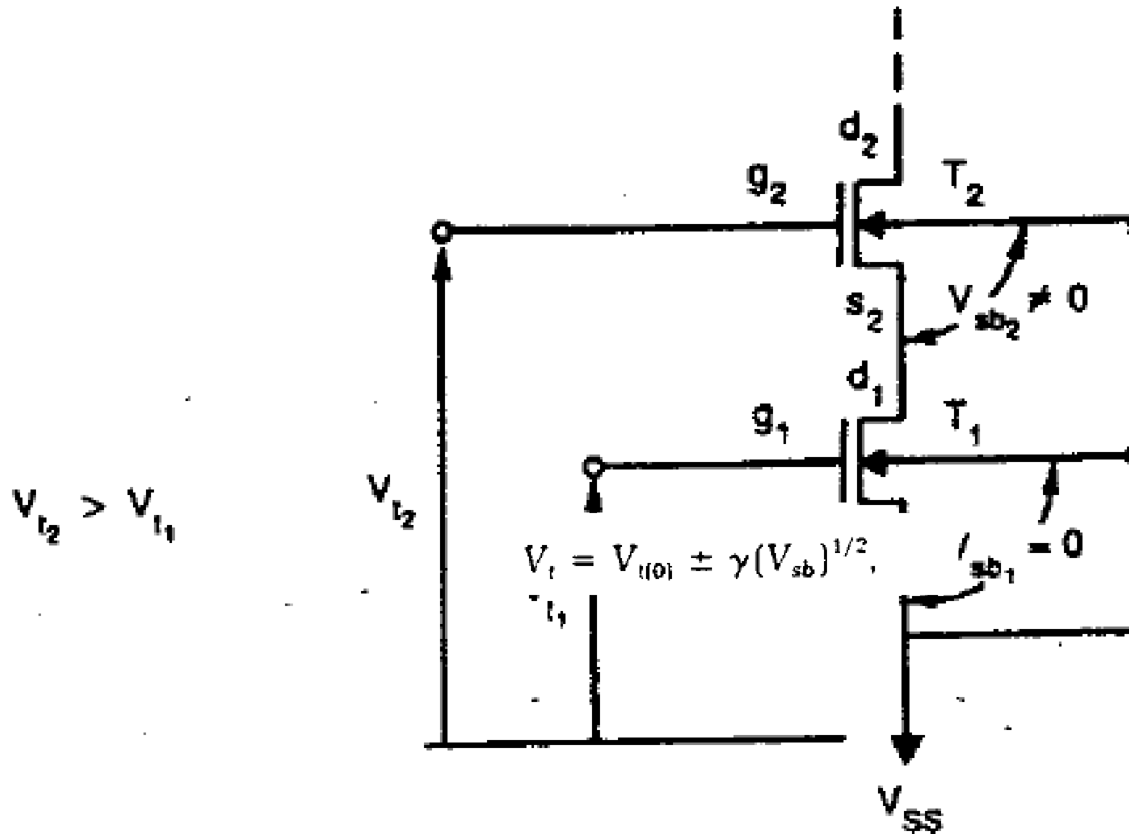
2 Methods

1.By varying doping concentration at silicon – insulator interface through ion implantation

2.Using different insulating material for gate

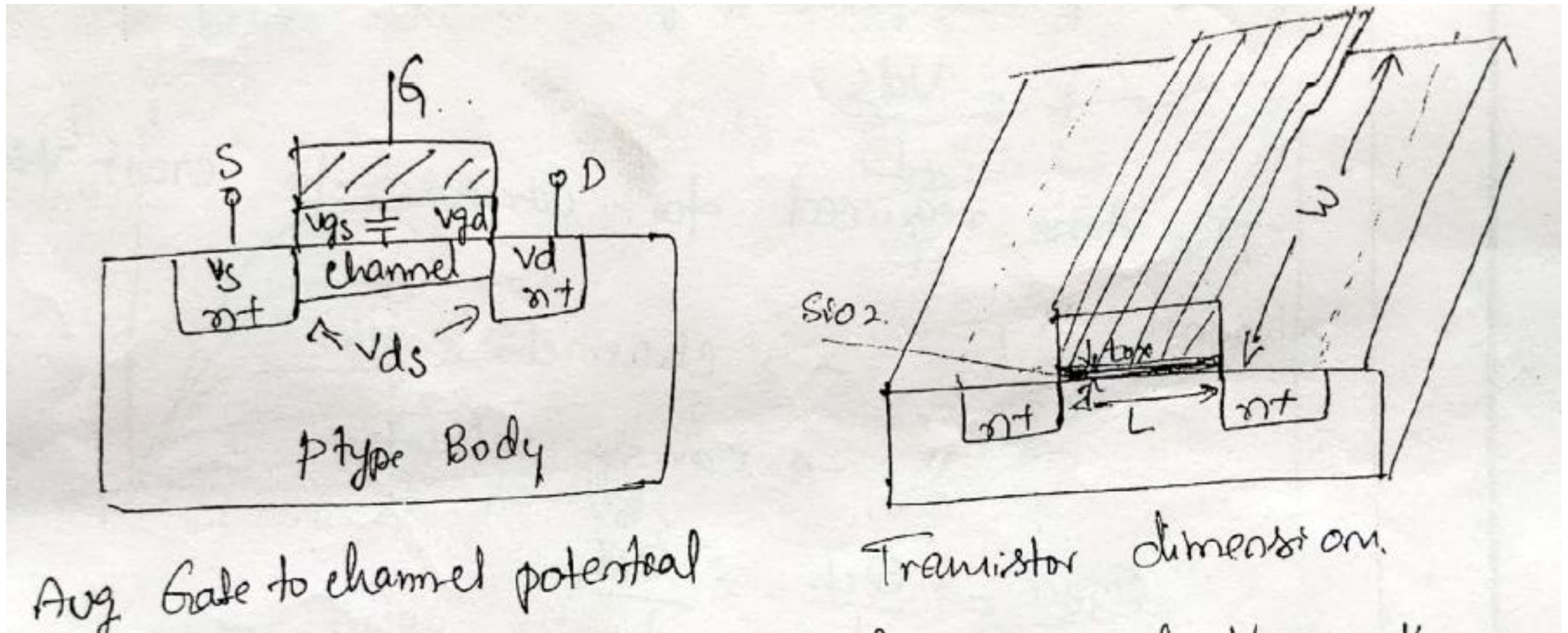
Ex Silicon Nitride combined with Silicon dioxide

# Body effect




$$V_t = V_{t(0)} \pm \gamma (V_{sb})^{1/2},$$

# Geometrical representation of NMOS



# NMOS device design equations

MOS transistors have 3 regions of operation namely

- cut-off region
- linear region
- saturation region.

The ideal (first order) equations [Cobb70][Sah64] describing the behavior of an nMOS device in the three regions are:

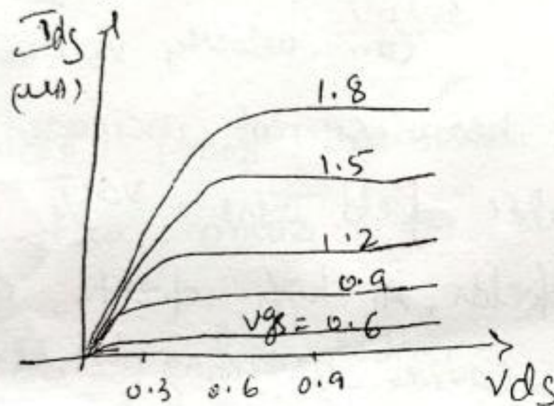
$$I_{ds} = \begin{cases} 0; & V_{gs} - V_t \leq 0 \quad \text{cut-off} \quad (a) \\ \beta\left[(V_{gs} - V_t)V_{ds} - \dfrac{V_{ds}^2}{2}\right]; & 0 < V_{ds} < V_{gs} - V_t \quad \text{linear} \quad (b) \\ \dfrac{\beta}{2}(V_{gs} - V_t)^2; & 0 < V_{gs} - V_t < V_{ds} \quad \text{saturation} \quad (c), \end{cases} \quad (2.2)$$

# Summary

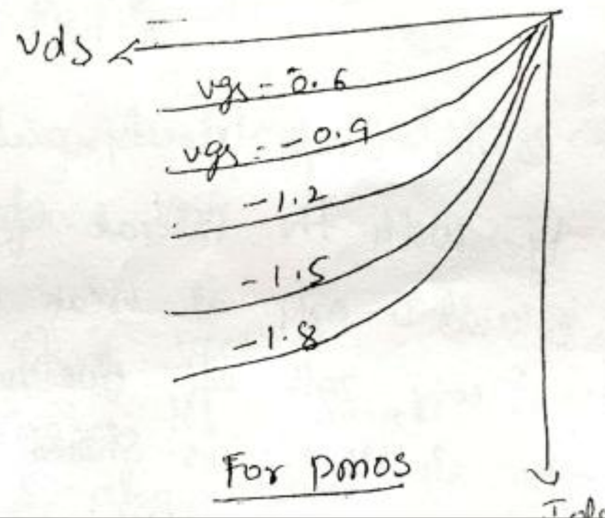
Summary

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta\left(V_{gs} - V_t - \frac{V_{ds}}{2}\right)V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \frac{\beta}{2}(V_{gs} - V_t)^2 & V_{ds} > V_{dsat} & \text{Saturation} \end{cases}$$

Fig below shows IV char of transistor

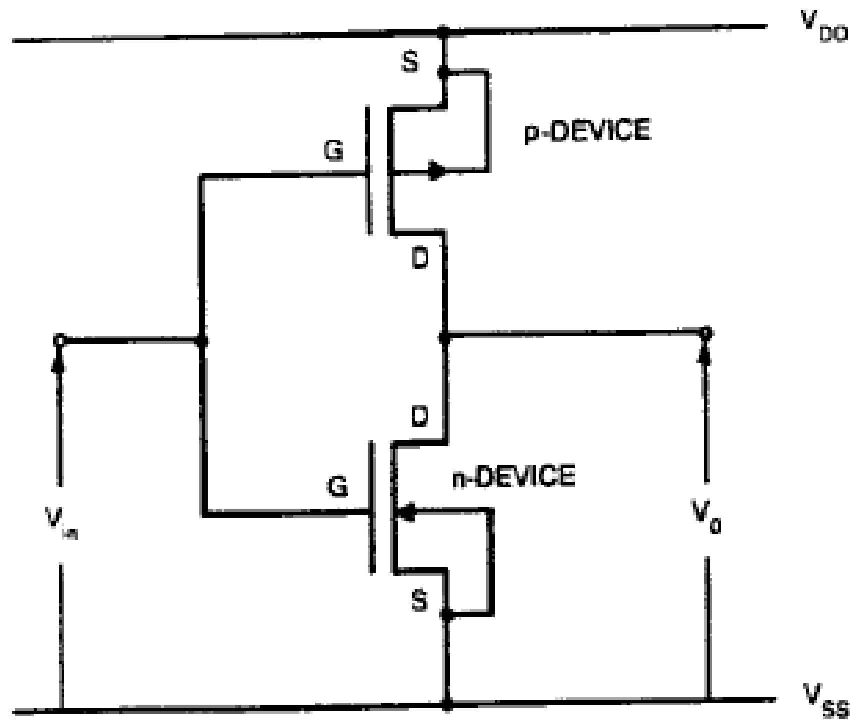



For nmos

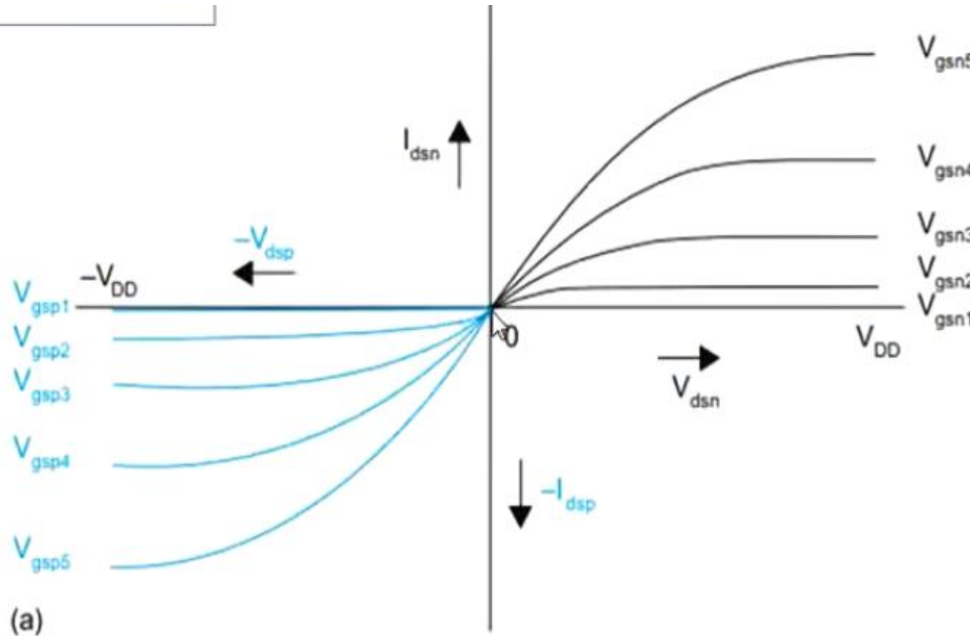


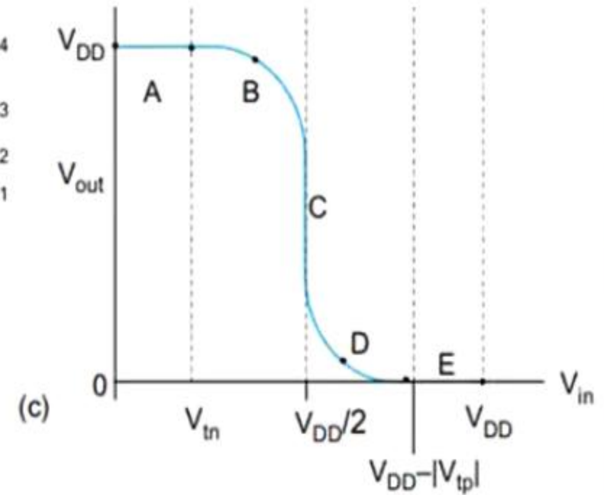

For pmos

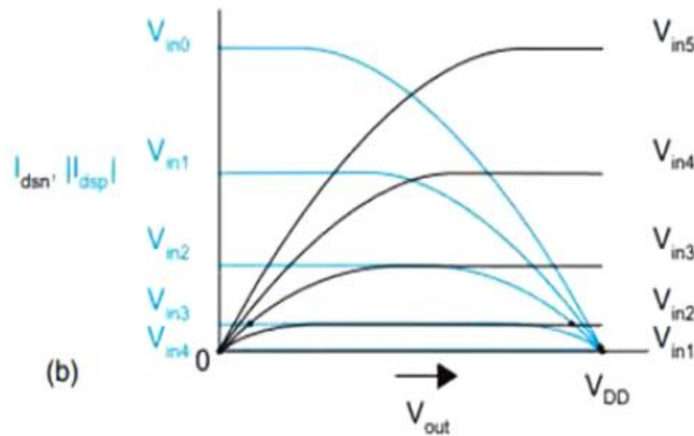
# CMOS Inverter

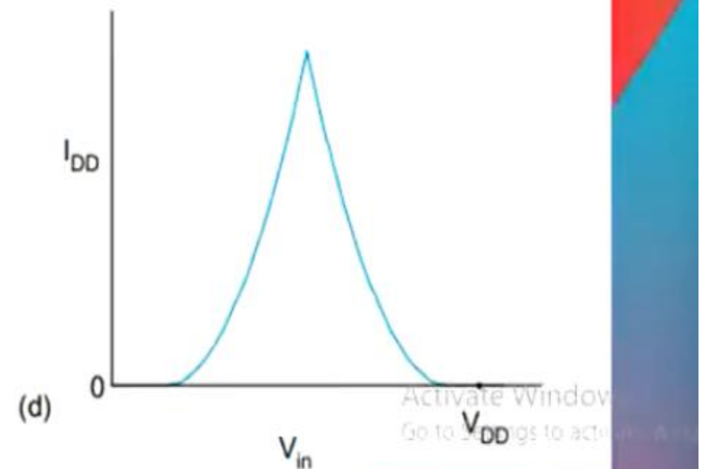


# Graphical representation of inverter characteristics

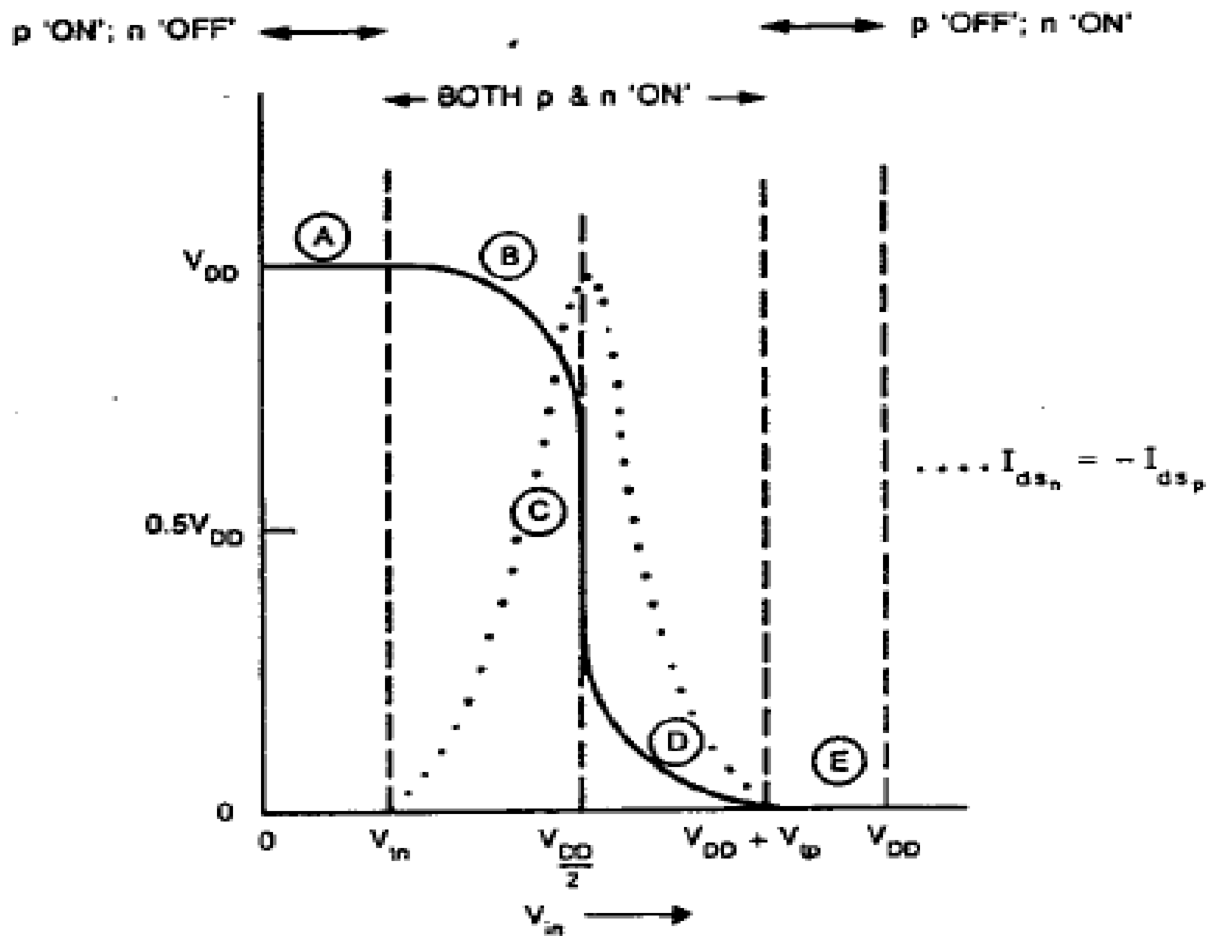


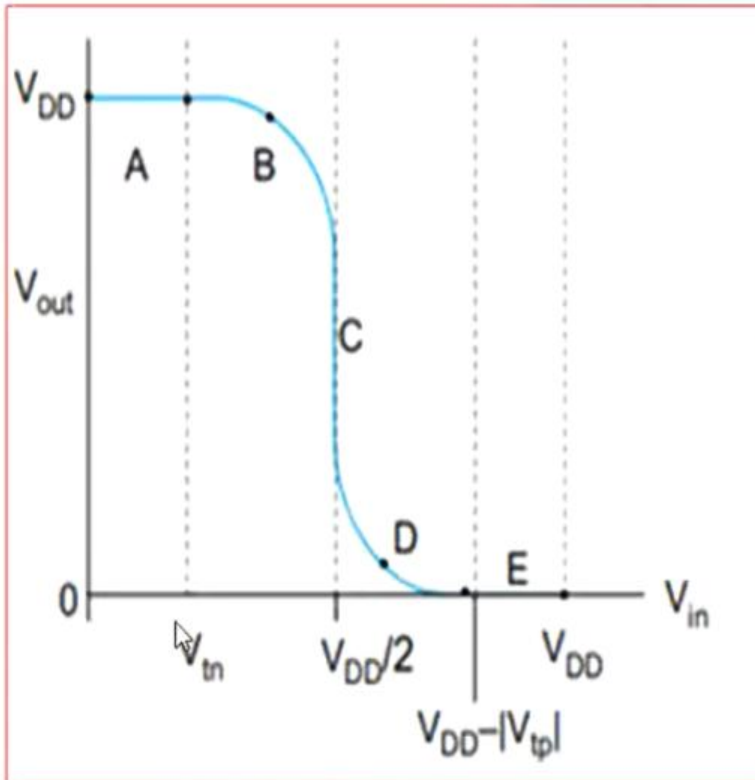



# DC Transfer characteristics of CMOS Inverter






| | Cutoff | Linear | Saturated |
|---|---|---|---|
| nMOS | $V_{gsn} < V_{tn}$ | $V_{gsn} > V_{tn}$ | $V_{gsn} > V_{tn}$ |
| | $V_{in} < V_{tn}$ | $V_{in} > V_{tn}$ | $V_{in} > V_{tn}$ |
| | | $V_{dsn} < V_{gsn} - V_{tn}$ | $V_{dsn} > V_{gsn} - V_{tn}$ |
| | | $V_{out} < V_{in} - V_{tn}$ | $V_{out} > V_{in} - V_{tn}$ |
| pMOS | $V_{gsp} > V_{tp}$ | $V_{gsp} < V_{tp}$ | $V_{gsp} < V_{tp}$ |
| | $V_{in} > V_{tp} + V_{DD}$ | $V_{in} < V_{tp} + V_{DD}$ | $V_{in} < V_{tp} + V_{DD}$ |
| | | $V_{dsp} > V_{gsp} - V_{tp}$ | $V_{dsp} < V_{gsp} - V_{tp}$ |
| | | $V_{out} > V_{in} - V_{tp}$ | $V_{out} < V_{in} - V_{tp}$ |

| Region | Condition | p-device | n-device | Ou |
|---|---|---|---|---|
| A | $0 \le V_{in} < V_{tn}$ | linear | cutoff | $V_{out} = V_D$ |
| B | $V_{tn} \le V_{in} < V_{DD}/2$ | linear | saturated | $V_{out} > V_D$ |
| C | $V_{in} = V_{DD}/2$ | saturated | saturated | $V_{out}$ drop |
| D | $V_{DD}/2 < V_{in} \le V_{DD} - \|V_{tp}\|$ | saturated | linear | $V_{out} < V_D$ |
| E | $V_{in} > V_{DD} - \|V_{tp}\|$ | cutoff | linear | $V_{out} = 0$ |

# Summary

Summary

| Region | condition | P Device | N Device | output |
|---|---|---|---|---|
| A | $0 \le V_{in} \le V_{tn}$ | Linear | cutoff | $V_{out} = V_{DD}$ |
| B | $V_{tn} \le V_{in} < \frac{V_{DD}}{2}$ | Linear | Saturated | $V_{out} > \frac{V_{DD}}{2}$ |
| C | $V_{in} = \frac{V_{DD}}{2}$ | Saturated | Saturated | $V_{out}$ drops |
| D | $\frac{V_{DD}}{2} < V_{in} < V_{DD} - \lvert V_{tp} \rvert$ | Saturated | Linear | $V_{out} < \frac{V_{DD}}{2}$ |
| E | $V_{in} > V_{DD} - \lvert V_{tp} \rvert$ | cutoff | Linear | $V_{out} = 0$ |

# Beta (β) Ratio Effect

$$I_{dsp} = \frac{\beta_p}{2}(V_{in} - V_{DD} - V_{tp})^2$$

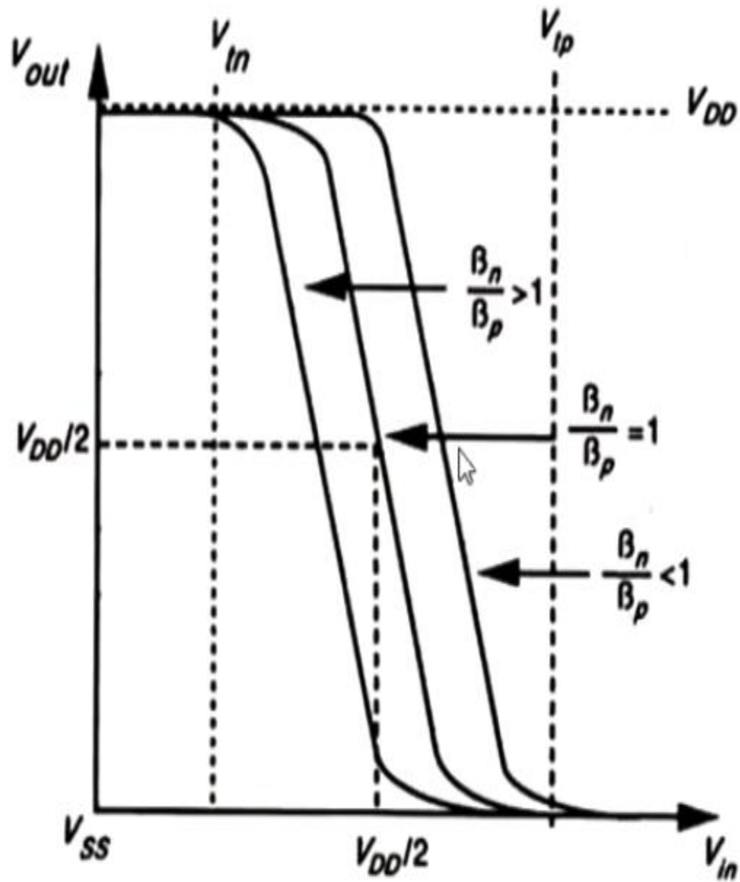
$$\beta = K\frac{W}{L}$$

$$I_{dsn} = \frac{\beta_n}{2}(V_{in} - V_{tn})^2$$

$$K = \frac{\varepsilon_{ins}\varepsilon_0\mu}{D}$$

$\mu_n \doteq 650\ cm^2/V\ sec$ (surface)

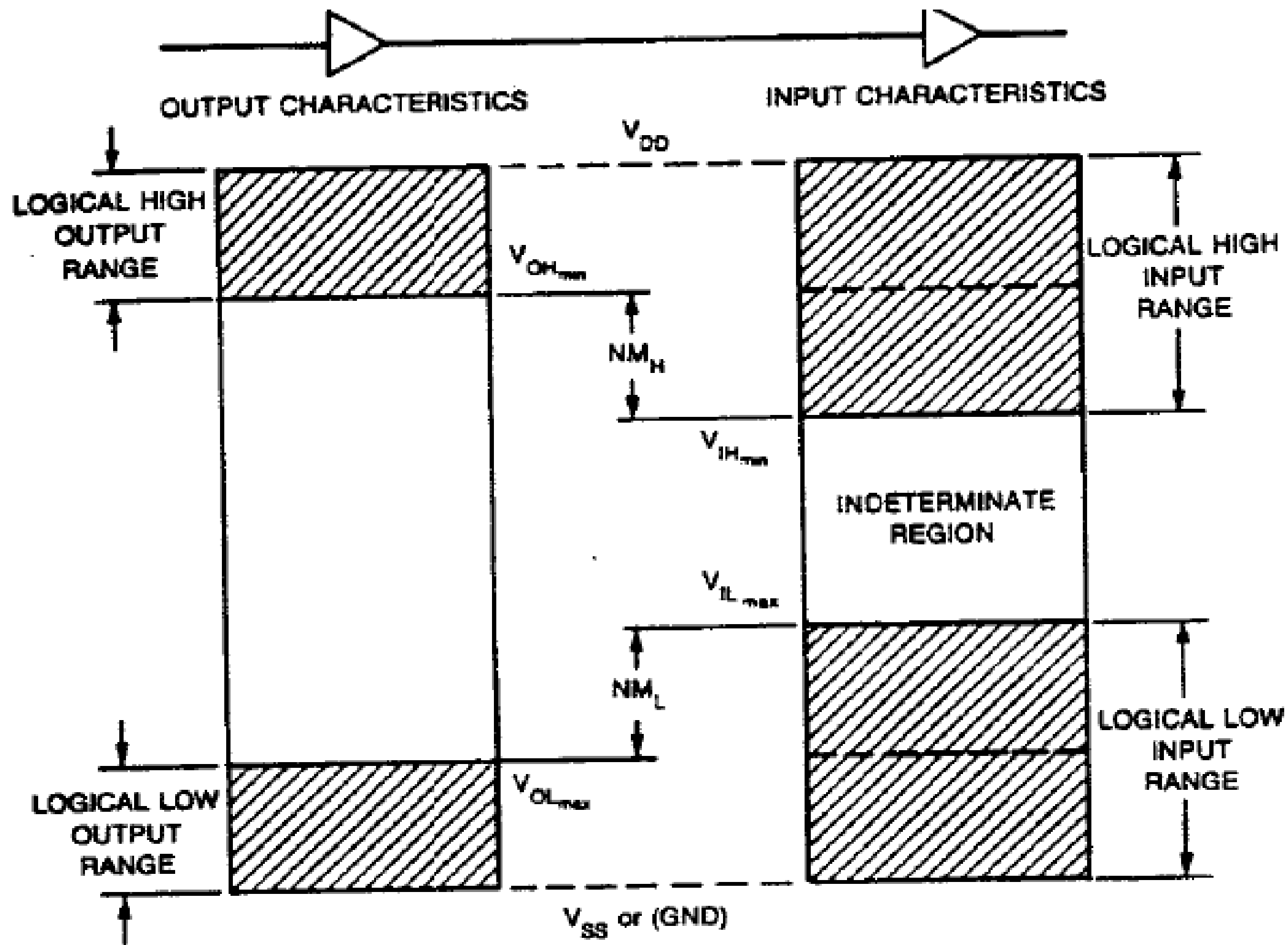
$\mu_p \doteq 240\ cm^2/V\ sec$ (surface)



# Noise Margin

- **Noise margin or Noise immunity is allowable input gate voltage so that output will not be corrupted.**
- NML is defined as difference in maximum LOW input voltage recognized by receiving gate and maximum low output voltage produced by the driving gate.
- **$NM_L$= VIL-VOL**
- NMH is defined as difference in minimum HIGH output voltage of driving gate and min HIGH input voltage recognized by receiving gate
- **$NM_H$=VOH -VIH**

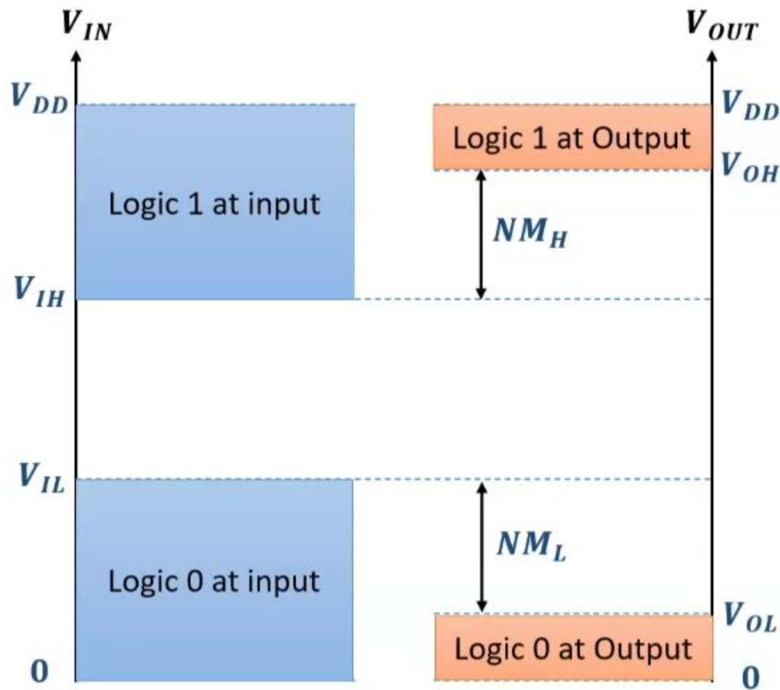
# Noise margin definitions

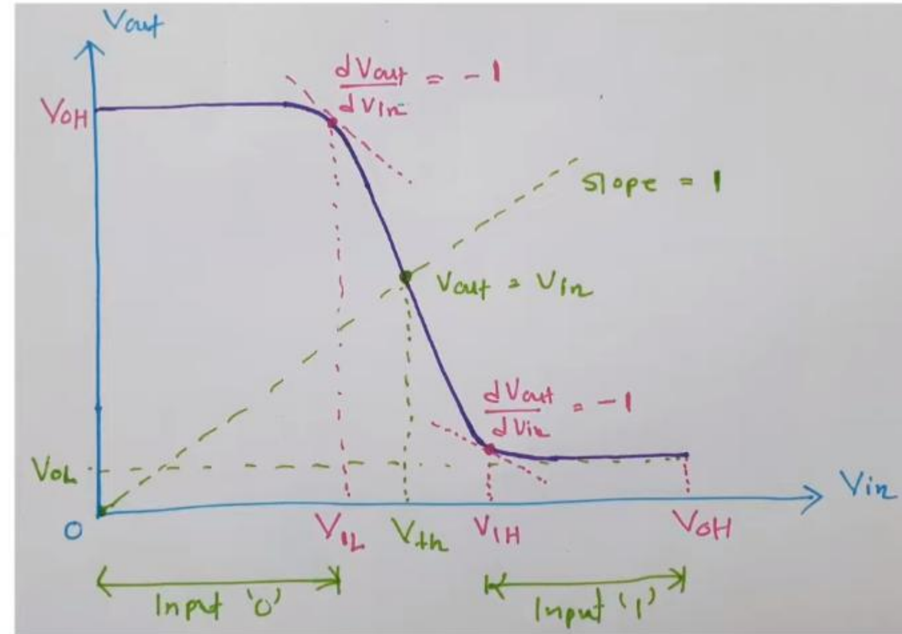


# Basics of Noise Margin

- It explains, up to what extent, IC allows noise in transmission of logic ‘0’ and logic ‘1’.
- In digital Integrated circuits, we don’t receives only two voltages. (One for logic ‘0’ and another for logic ‘1’).
- Here we receives range of voltages and we identify logic ‘0’ or ‘1’ based on it.
- Received voltage range widens based on noise in the circuit. So for error less transmission, noise margin is required.

# Noise Margin based on VTC of inverter

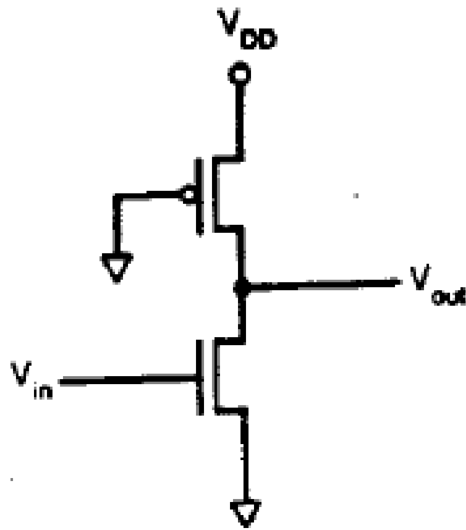


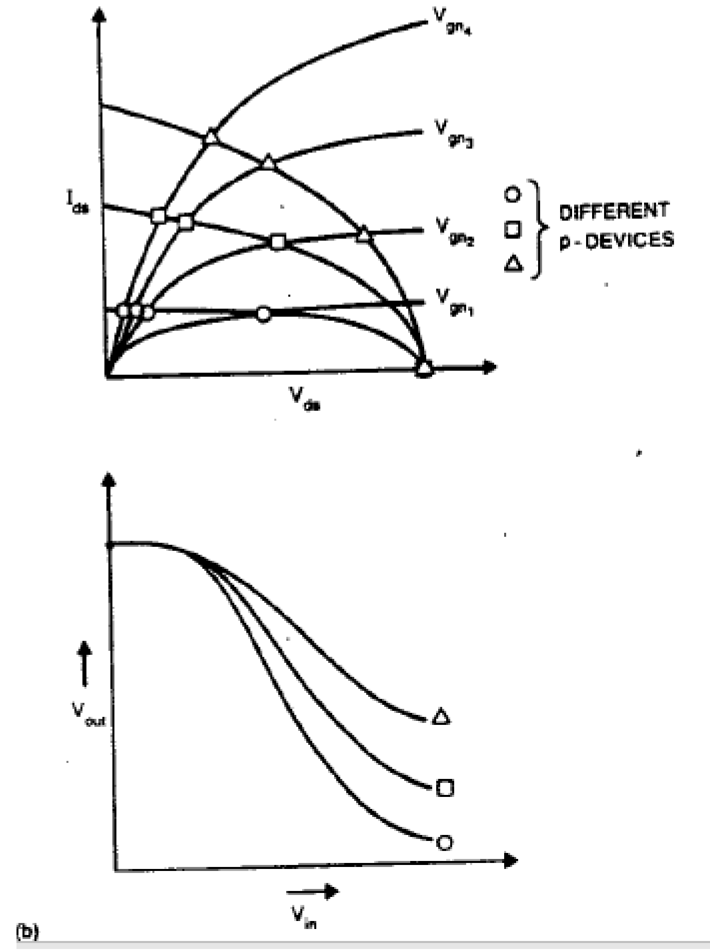




$$NM_H = V_{OH} - V_{IH}$$

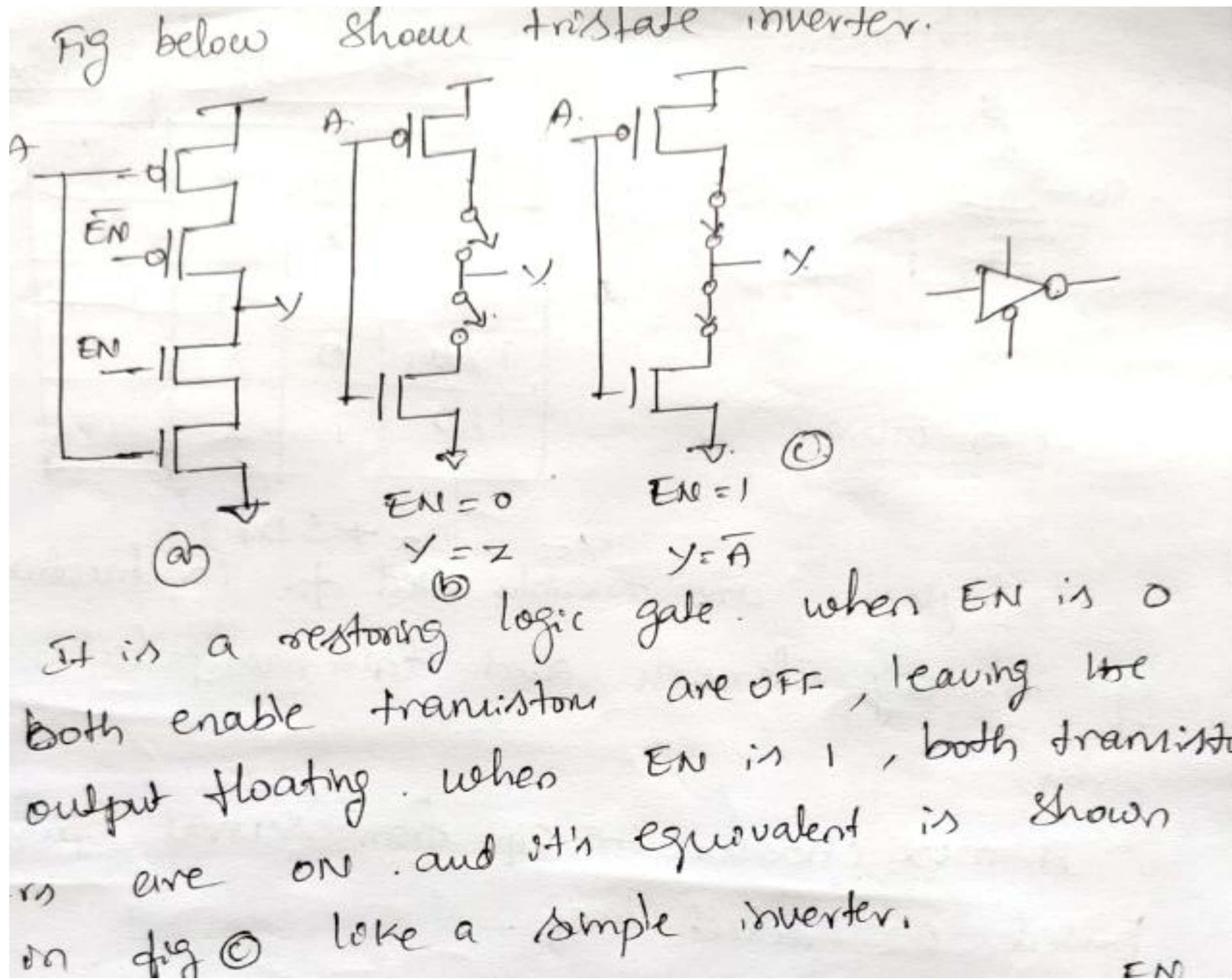
$$NM_L = V_{IL} - V_{OL}$$

# Alternate CMOS Inverters-Pseudo NMOS INV

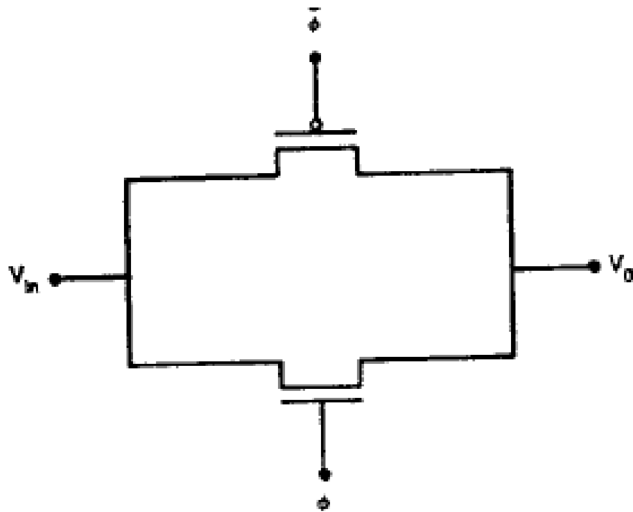


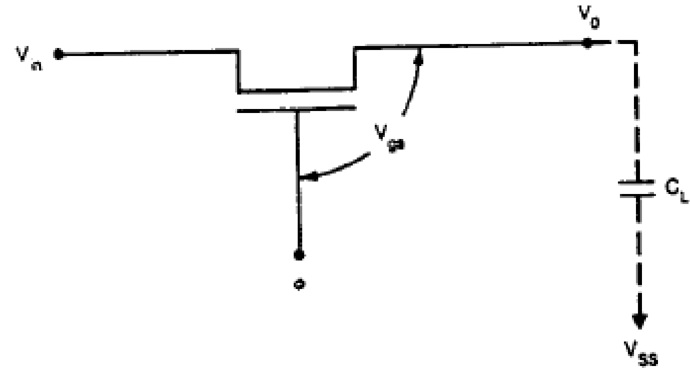



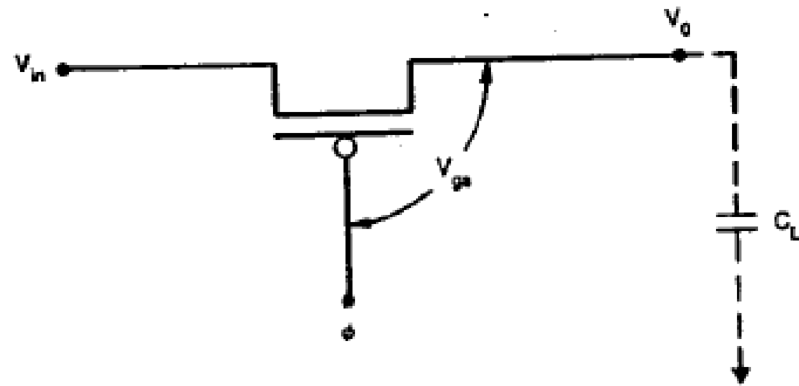
# Tristate Inverter



# TG-DC characteristics



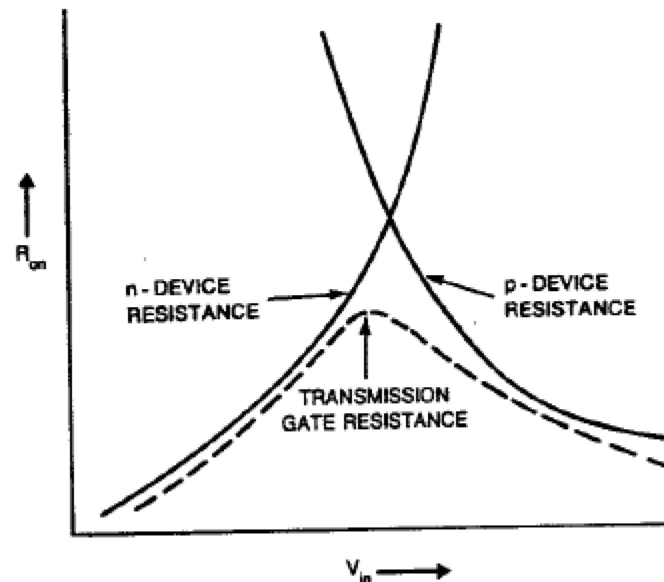



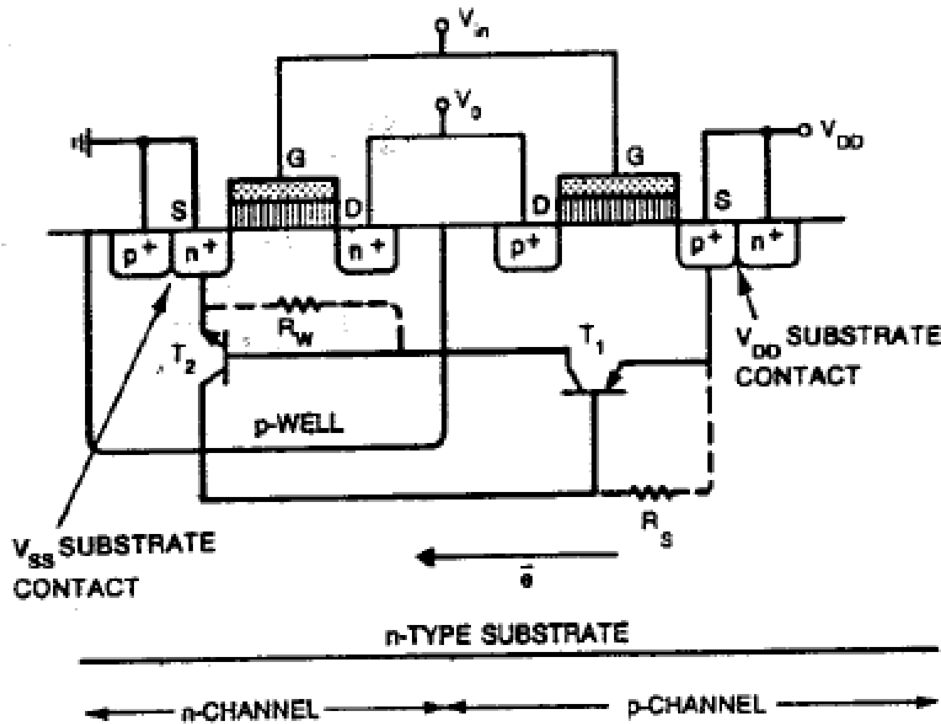
$$\phi = \text{'0'}; \begin{cases} \text{n-device} = \text{off}; \\ \text{p-device} = \text{off}; \\ V_{in} = \text{'0'}, V_O = Z; \\ V_{in} = \text{'1'}, V_O = Z, \end{cases}$$

where $Z$ refers to a high impedance state and

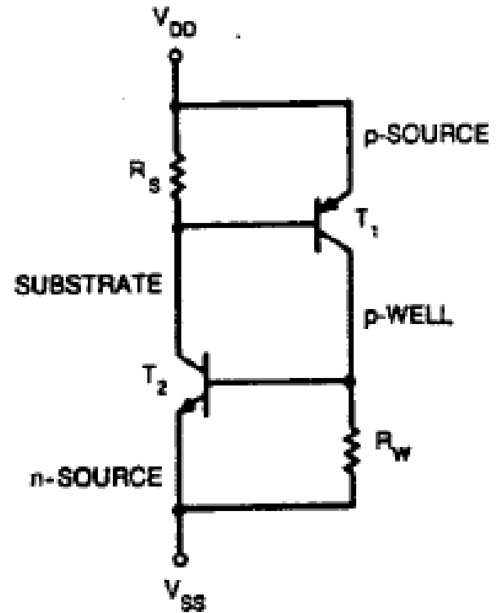
$$\phi = \text{'1'}; \begin{cases} \text{n-device} = \text{on}; \\ \text{p-device} = \text{on} \\ V_{in} = \text{'0'}, V_O \\ V_{in} = \text{'1'}, V_O \end{cases}$$



# Latch up




(a) CROSS SECTION




(b) EQUIVALENT CIRCUIT FOR PARASITIC TRAN.

# Definition-Latch up

- **Latch-up in CMOS VLSI** refers to an unintended low-impedance path that can occur between the VDD and VSS resulting in high current that can damage the circuit or cause it to malfunction. This phenomenon occurs when parasitic structures within the CMOS circuitry (such as parasitic bipolar transistors) become inadvertently activated, leading to a short circuit.

# Steps to avoid latchup problem

- Here's a summarized list of steps to avoid latch-up in CMOS VLSI designs:

- **Proper Layout Design**: Avoid placing PMOS and NMOS transistors close enough to create parasitic bipolar transistors.
- **Use Guard Rings**: Implement guard rings around sensitive areas (e.g., inputs and outputs) to prevent latch-up.
- **Increase Well Spacing**: Maintain adequate distance between N-well and P-well to prevent parasitic SCR structures.
- **Use ESD Protection**: Design with electrostatic discharge (ESD) protection to prevent transient voltages triggering latch-up.
- **Control Supply Voltage**: Keep supply voltage stable and within safe limits, using decoupling capacitors to smooth voltage spikes.

- **Ensure Proper Power Sequencing**: Implement controlled power-on and power-off sequences for VDD and VSS.
- **Utilize Latch-up Immunity Features**: Leverage advanced CMOS process features that enhance latch-up resistance.
- **Consider BiCMOS Technology**: For high-speed or mixed-signal applications, consider using BiCMOS technology for improved latch-up immunity.
- **Simulate for Latch-up**: Use simulation tools to detect and address latch-up vulnerabilities during the design phase.
- **Monitor Temperature**: Ensure the design operates within temperature limits to prevent latch-up due to thermal effects.