VLSI DESIGN AND TESTING (BEC602)

Padmavathi N

Associate Professor

Department of ECE

Course objectives

1.This course deals with analysis and design of digital CMOS integrated circuits.

2. The course emphasizes on basic theory of digital circuits, design principles and techniques for

digital design blocks implemented in CMOS technology.

3. This course will also cover switching characteristics of digital circuits along with delay and power estimation.

4. Understanding the CMOS sequential circuits and memory design concepts.

5.Explore the knowledge of VLSI Design flow and Testing

Course Outcomes (COs)

- **After completing the course, the students will be able to**

CO1 -Apply the fundamentals of semiconductor physics in MOS transistors and analyze the geometrical effects of MOS transistors

CO2- Design and realize combinational, sequential digital circuits and memory cells in CMOS logic.

CO3- Analyze the synchronous timing metrics for sequential designs and structured design basics.

CO4- Understand designing digital blocks with design constraints such as propagation delay and dynamic power dissipation.

C05 -Understand the concepts of Sequential circuits design and VLSI testing

Text Books

- 1. Principals of CMOS VLSI Design A System approach Neil H E Weste and Kamran Eshraghain . Addition Wisley Publishing company.
- 2. “CMOS Digital Integrated Circuits: Analysis and Design”, Sung Mo Kang & Yosuf Leblebici, Third Edition, Tata McGraw-Hill.

Module 1 Syllabus

- **Introduction to CMOS Circuits:** Introduction, MOS Transistors, MOS Transistor switches, CMOS Logic, Alternate Circuit representation, CMOS-nMOS comparison.
- [Text 1: 1.1,1.2,1.3,1.4,1.5.1.6.]

Module 2 Syllabus

- **MOS Transistor Theory:** n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage,
- Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS
- inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin,
- Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.
- [Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.]

Module3 Syllabus

- **MOS Transistor Theory:** n-MOS enhancement transistor, p-MOS transistor, Threshold Voltage,
- Threshold voltage adjustment, Body effect, MOS device design equations, V-I characteristics, CMOS
- inverter DC characteristics, Influence of βn / βp ratio on transfer characteristics, Noise margin,
- Alternate CMOS inverters. Transmission gate DC characteristics. Latch-up in CMOS.
- [Text 1: 2.1,2.2,2.3,2.4,2.5.2.6.]

Module 4 Syllabus

- **CMOS Circuit and Logic Design:** Introduction, CMOS Logic structures, CMOS Complementary logic,
- Pseudo n-MOS logic, Dynamic CMOS logic, Clocked CMOS Logic, Cascade Voltage Switch logic, Pass
- transistor Logic, Electrical and Physical design of Logic gates, The inverter, NAND and NOR gates, Body
- effect, Physical Layout of Logic gates, Input output Pads.
- [Text 1: 5.1,5.2,5.2.1, , 5.2.2, 5.2.3, 5.2.4, 5.2.6, 5.2.8, 5.3,5.3.1,5.3.2, 5.3.4 ,5.3.8,5.5]

Module 5 Syllabus

- **Sequential MOS Logic Circuits:** Introduction, Behaviour of Bistable Elements (Excluding
- Mathematical analysis) SR Latch Circuit, Clocked Latch and Flip-Flop Circuits, Clocked SR Latch,
- Clocked JK Latch.
- [Text2: 8.1, 8.2, 8.3, 8.4]
- **Structured Design and Testing:** Introduction**,** Design Styles, Testing
- [Text1: 6.1, 6.2. 6.5]

Contents

- *What is VLSI ?*
- *An Preview.*
- *VLSI World.*
- *Moore Law.*
- *VLSI Industry.*
- *Objective for VLSI Design.*
- *Applications.*
- *Future of VLSI.*

Indentify the Image

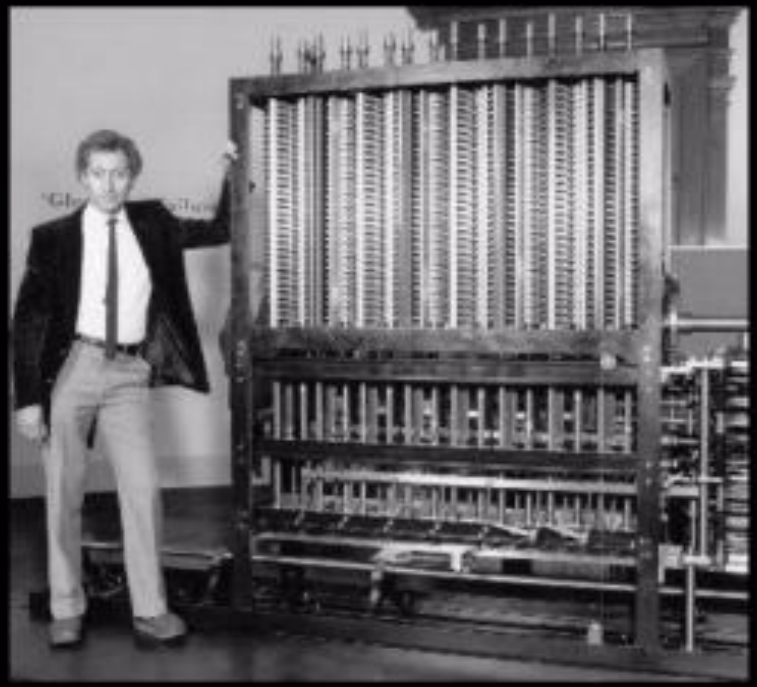
5 MB Hard Drive being Shipped by IBM - 1956.

This is Called VLSI Advancement !

5MB (IBM)-1956, Cost - $10,000/ 1 MB

4TB (WB)-2013

This achieved because of VLSI



Charles Babbage designed the first computer, starting in 1823

Unbelievable facts

AVIDAC was the first digital computer at Argonne National Laboratory, and began operating in 1953. It was built by the Physics Division for $250,000. Pictured shown AVIDAC, is pioneer Argonne computer scientist Jean F. Hall. AVIDAC stands for "Argonne Version of the Institute's Digital Automatic Computer" and was based on architecture developed by mathematician John von Neumann.

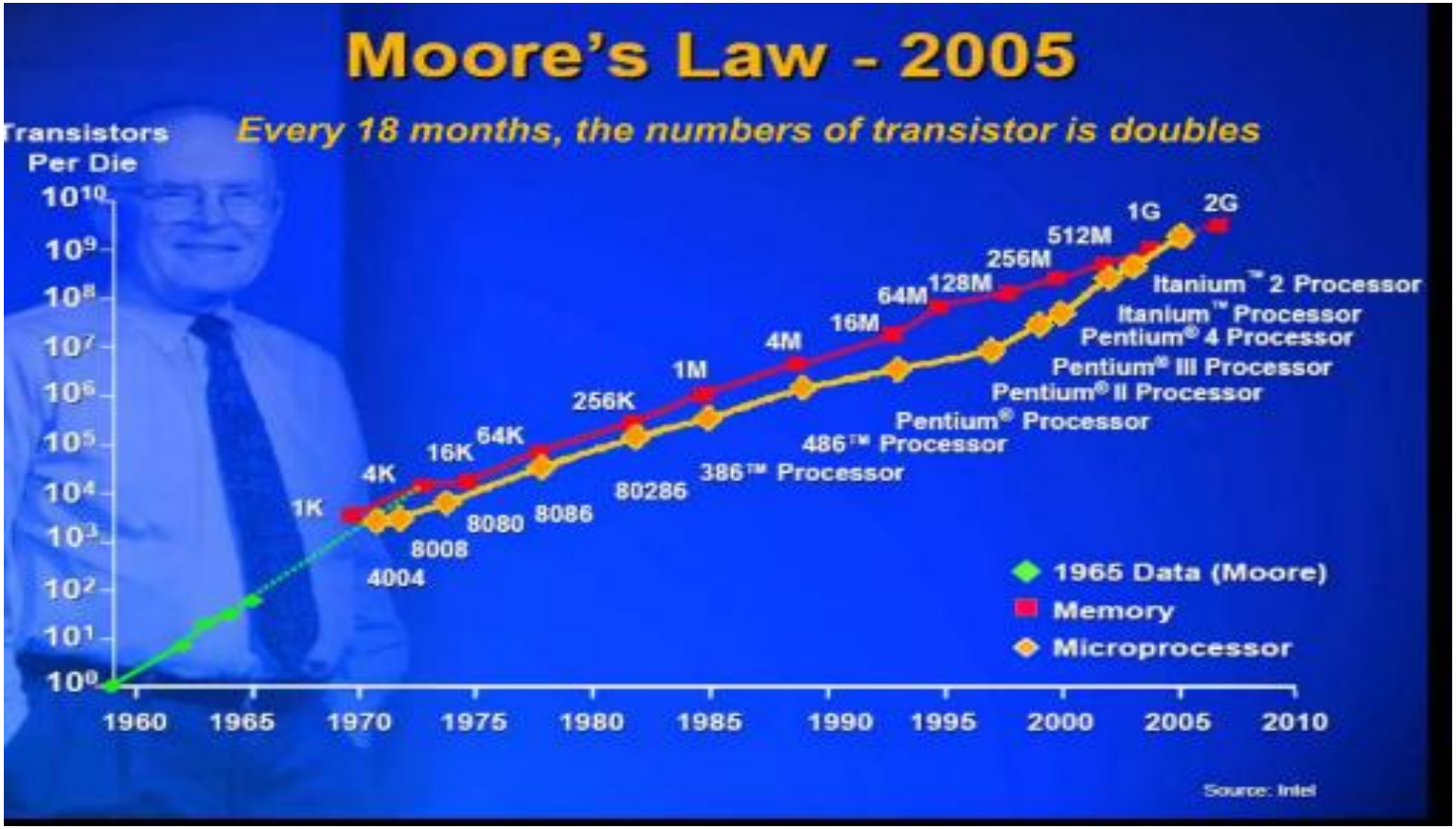
Apple Development

Apple I-1976

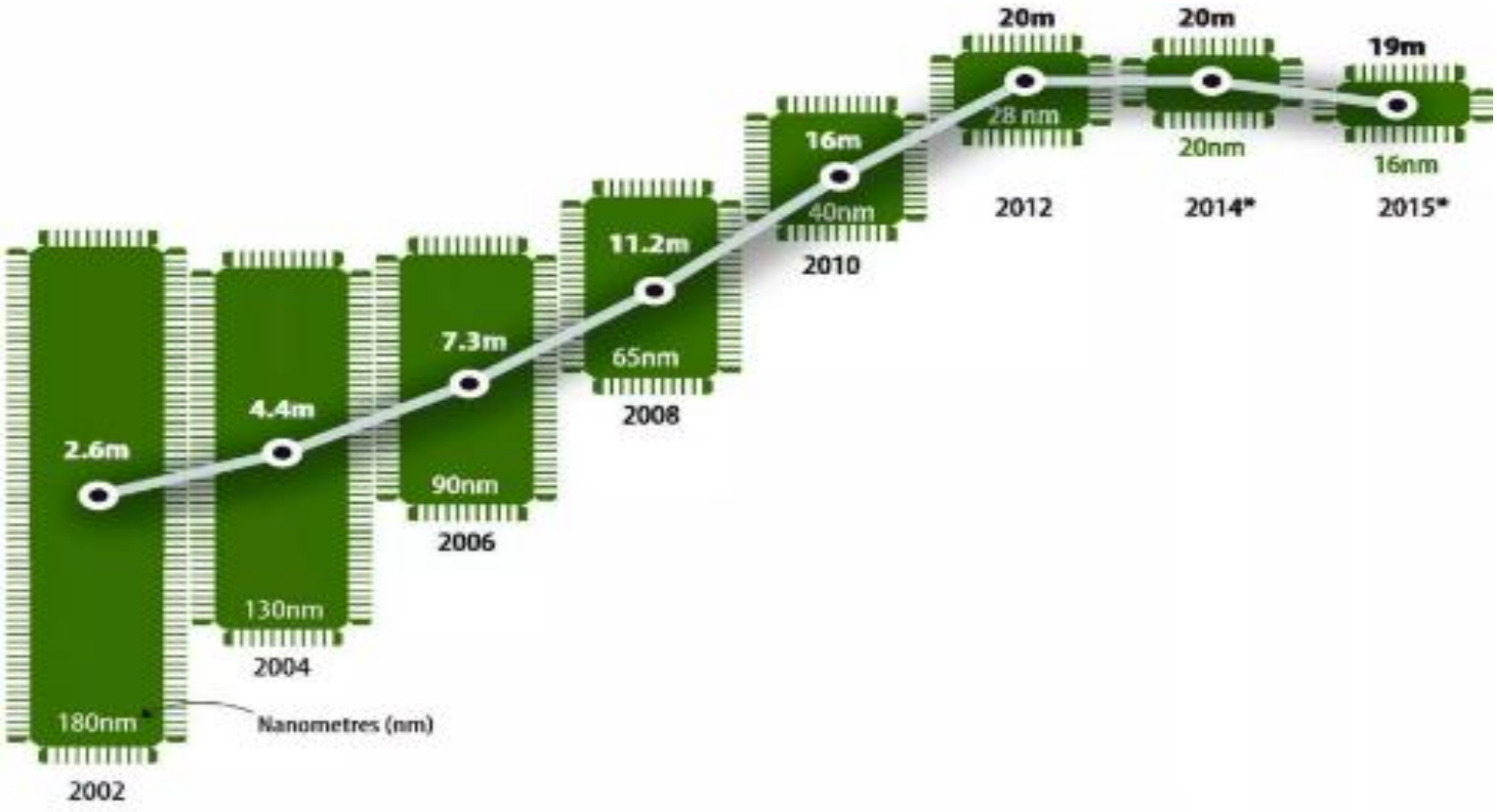
Apple- 2011

VLSI

- ***Very Large Scale Integration (within IC)***
- How large is Very Large?
  - ✓SSI (small scale integration)
    - ✓ 7400 series, 10-100 transistors
  - ✓MSI (medium scale)
    - ✓74000 series 100-1000
  - ✓LSI 1,000-10,000 transistors
  - ✓**VLSI > 10,000 transistors**
  - ✓ULSI/SLSI (Not so popular)


Moore's Law - 2005
Every 18 months, the numbers of transistor is doubles
Transistors Per Die
10^10
10^9
10^8
10^7
10^6
10^5
10^4
10^3
10^2
10^1
10^0
1960
1965
1970
1975
1980
1985
1990
1995
2000
2005
2010
1K
4K
16K
64K
256K
1M
4M
16M
64M
128M
256M
512M
1G
2G
4004
8008
8080
8086
80286
386™ Processor
486™ Processor
Pentium® Processor
Pentium® II Processor
Pentium® III Processor
Pentium® 4 Processor
Itanium™ Processor
Itanium™ 2 Processor
1965 Data (Moore)
Memory
Microprocessor
Source: Intel

Timeline

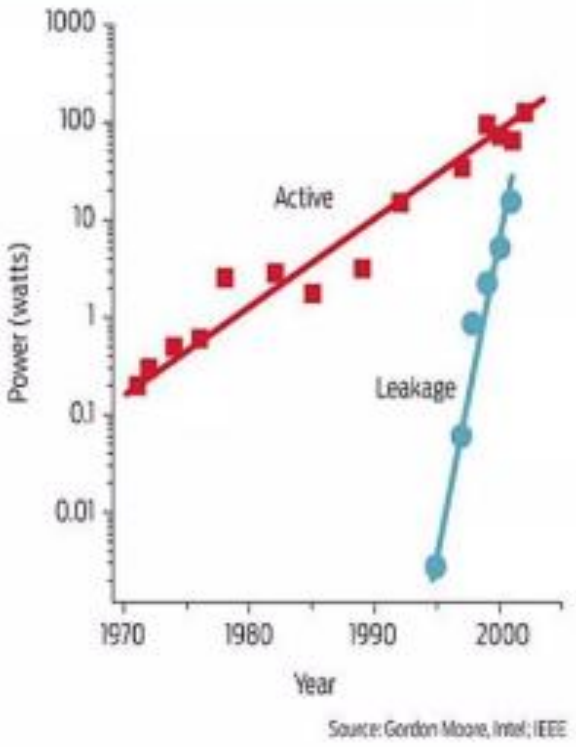

2.6m
180nm
2002
4.4m
130nm
2004
7.3m
90nm
2006
11.2m
65nm
2008
16m
40nm
2010
20m
28 nm
2012
20m
20nm
2014*
19m
16nm
2015*
Nanometres (nm)

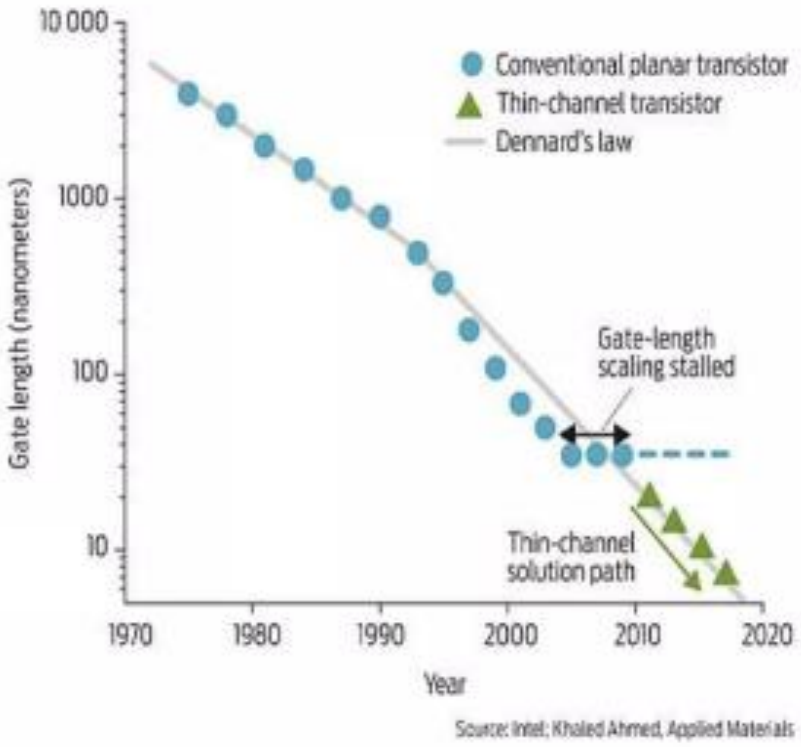
Timeline of Electronic Devices

Now a Days 2000-2016>> Sensor, Transducer integrated on SOCs

Entered to Nanotechnology

Power and Size





Sizes of VLSI Chip

- *In 20nm transistors, you can fit around 250 billion of them on a silicon wafer around the size of a fingernail.*

- iPad Air 2 has a custom tri-core ARM CPU and custom octa-core PowerFX GPU, for a total of 3 billion transistors on-die.

VLSI Companies In India

VLSI COMPANIES IN INDIA

- Analog Devices India Product Development Center – Designs DSPs in Bangalore
- Bit Mapper – Design, development & training
- CG-CoreEl Programmable Solutions – Design services in telecommunications, networking and DSP
- Calorex Institute of Technology – Courses in VLSI chip design, DSP and Verilog HDL
- ControlNet India – VLSI design, network monitoring products and services
- Cypress Semiconductor – US semiconductor major Cypress has set up a VLSI development center in Bangalore
- Delsoft – Electronic design automation, digital video technology and VLSI design services
- E Infochips – ASIC chip design, embedded systems and software development
- EDAIndia – Resource on VLSI design centres and tutorials
- Horizon Semiconductors – ASIC, VLSI and IC design training
- Microchip Technology – Offers VLSI CMOS semiconductor components for embedded systems
- Motorola India – IC design center
- Sandeepani – VLSI design training courses
- Sanyo LSI Technology – Semiconductor design centre of Sanyo Electronics
- Semiconductor Complex – Manufacturer of microelectronics equipment like VLSIs & VLSI based systems & sub systems

CMOS LOGIC

- **What is CMOS?**
  - Complementary Metal-Oxide-Semiconductor logic.
  - Uses both NMOS and PMOS transistors to implement logic functions.
- **Advantages of CMOS Logic:**
  - Low power consumption (no current flow when stable state).
  - High noise immunity.
  - Scalability and integration (large-scale integration, LSI).
- **Basic Logic Gates in CMOS:**
  - NOT, AND, OR, NAND, NOR, XOR, XNOR.

MOS Transistors-NMOS and PMOS

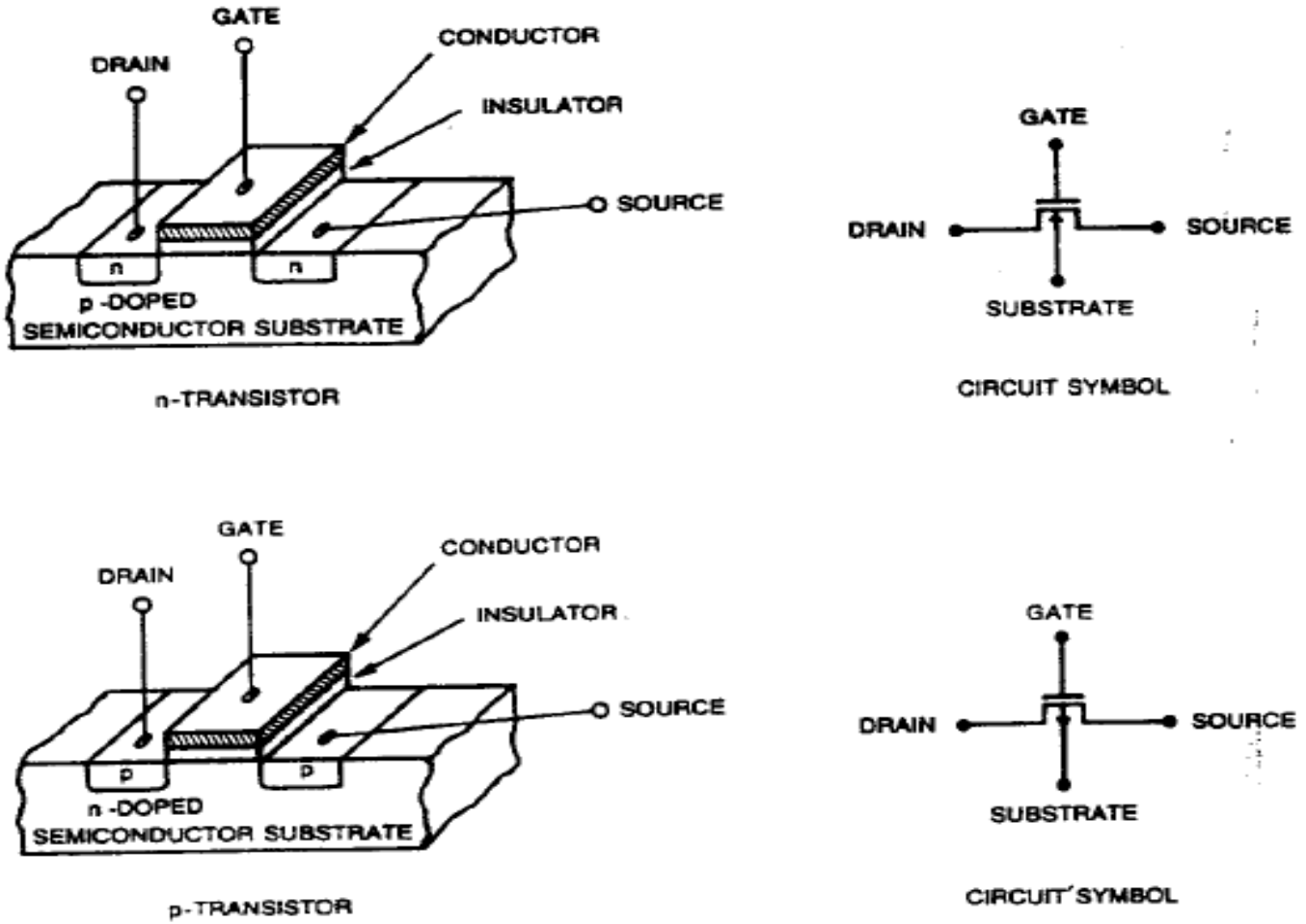


FIGURE 1.1. MOS transistor physical structures

MOS Transistor switches

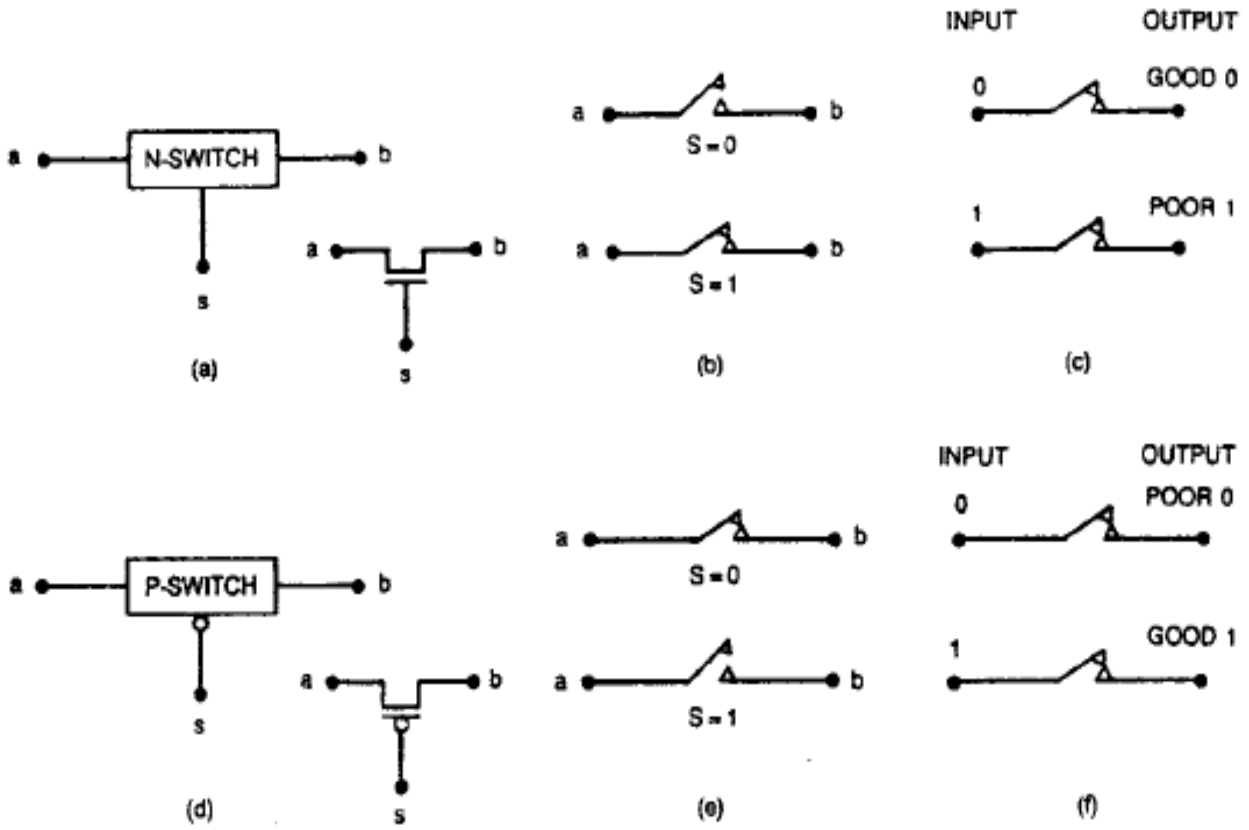
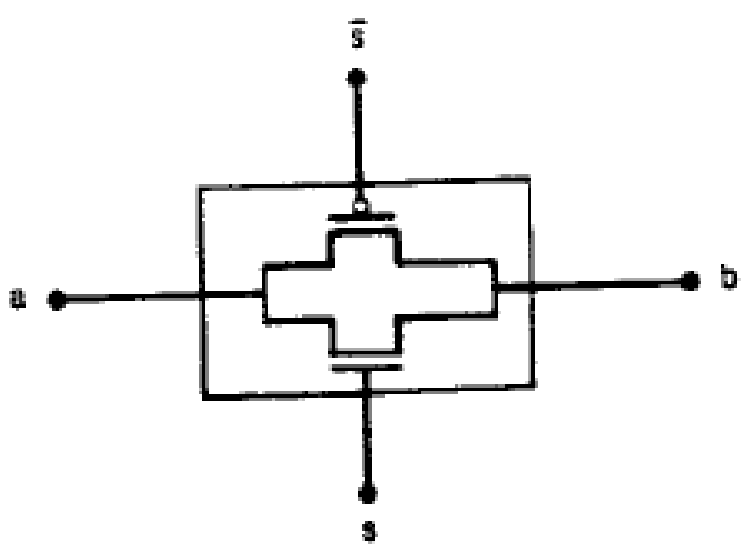
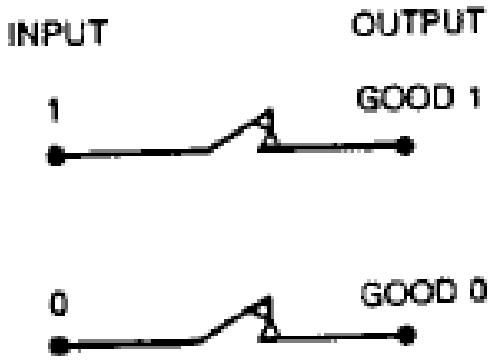
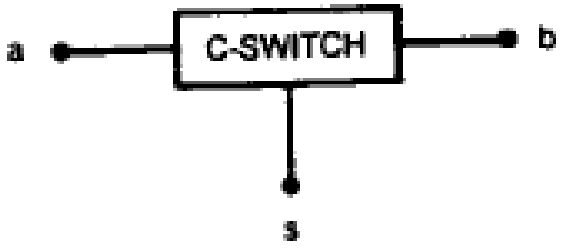


FIGURE 1.2. MOS transistors viewed as switches

Complementary Switch-C switch







CMOS Logic-Inverter

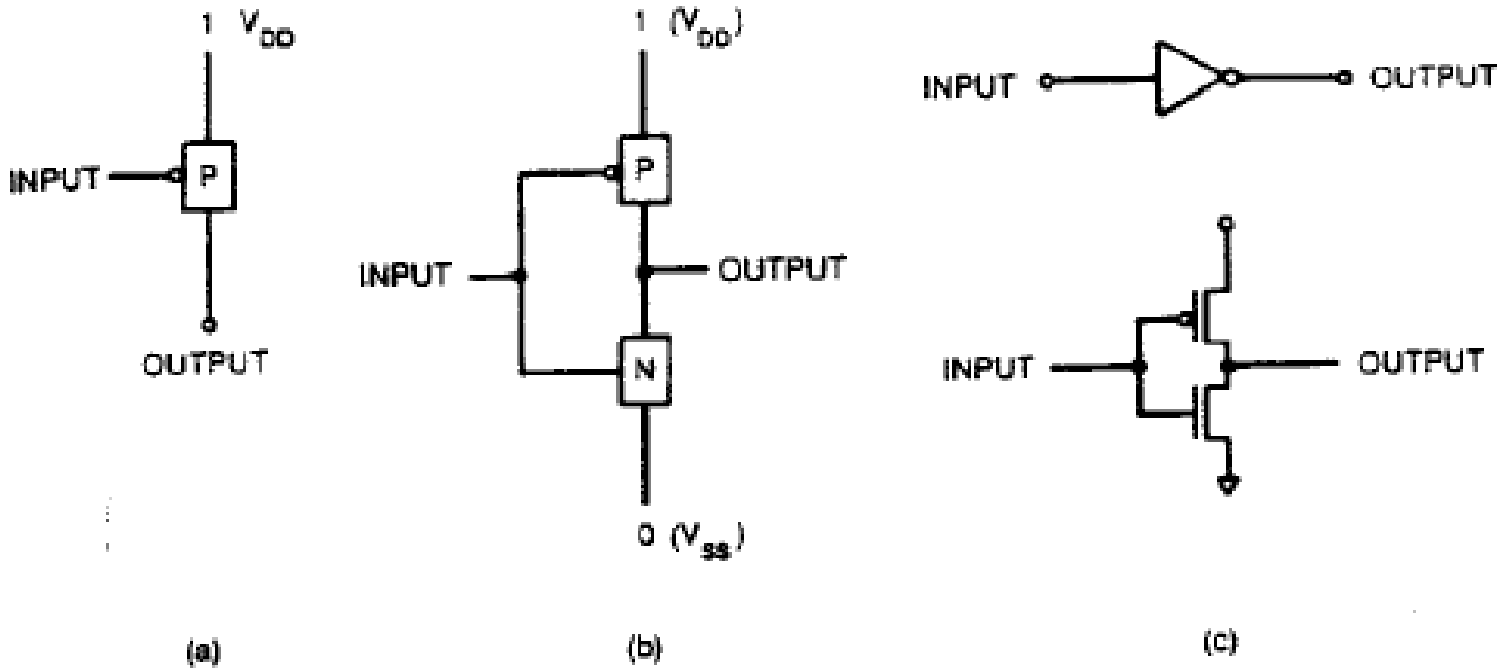
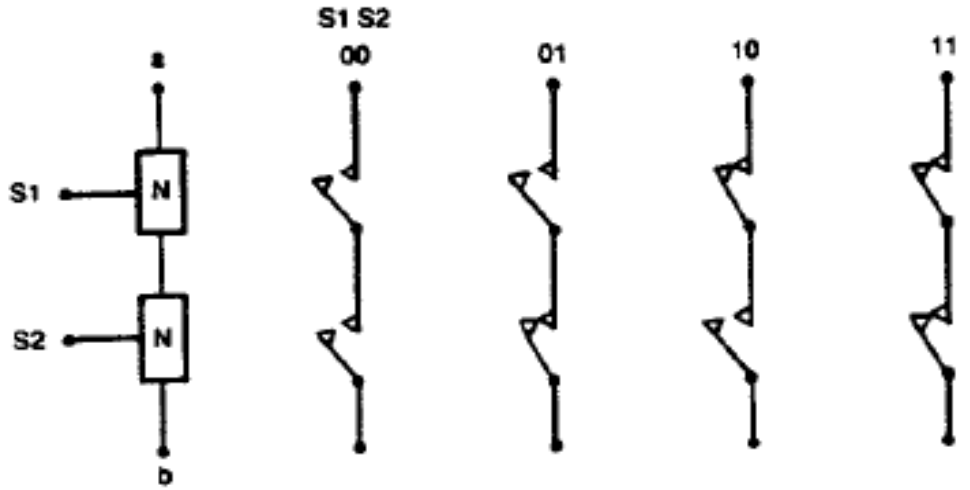
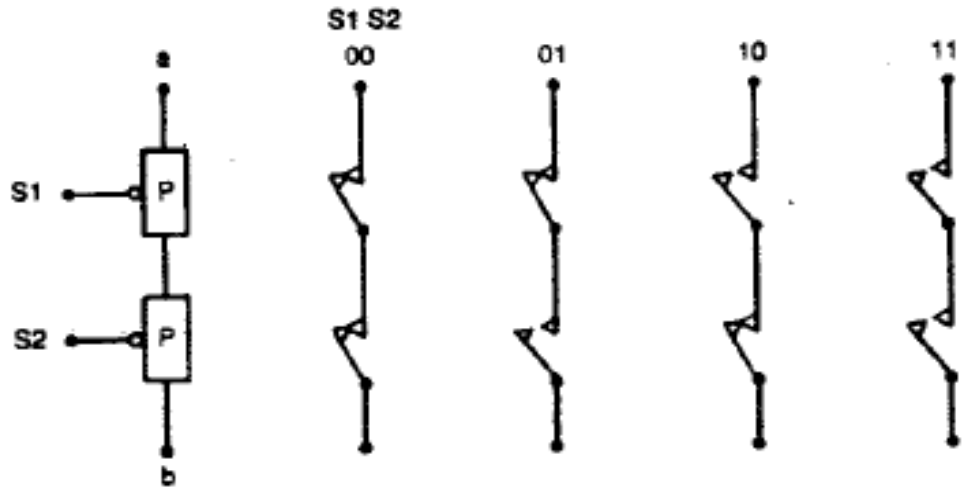


FIGURE 1.4. Construction of a CMOS inverter

Combinational Logic-Series switches

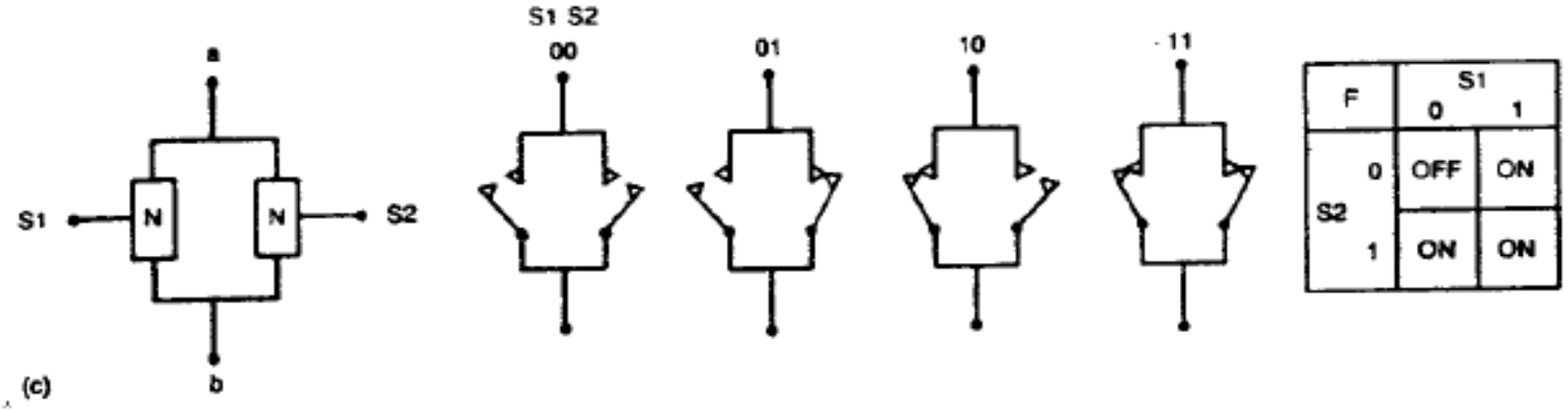


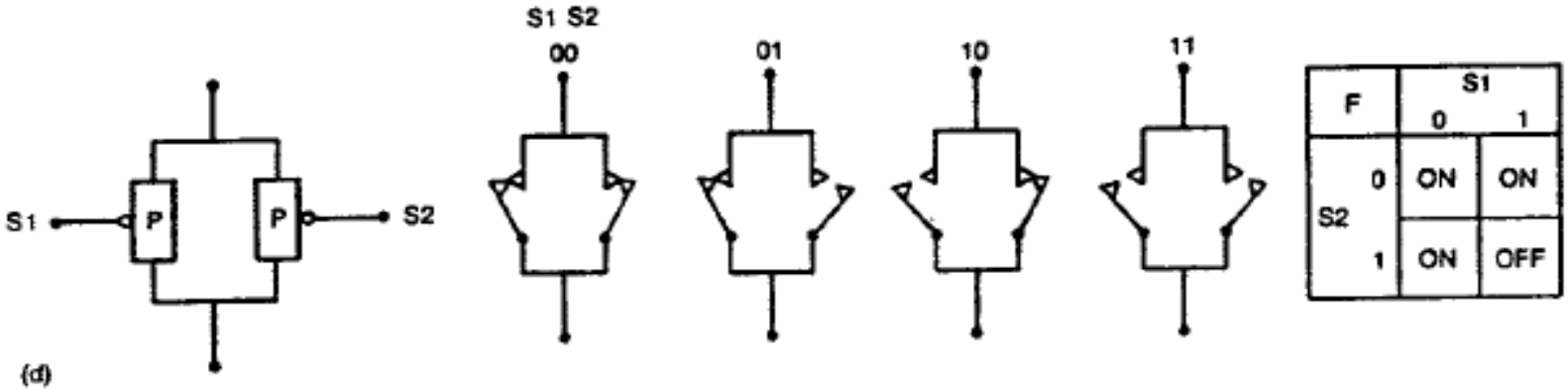
F	S1 0	S1 1
S2 0	OFF	OFF
S2 1	OFF	ON



F	S1 0	S1 1
S2 0	ON	OFF
S2 1	OFF	OFF

Combinational Logic-Parallel switches





CMOS NAND Gate

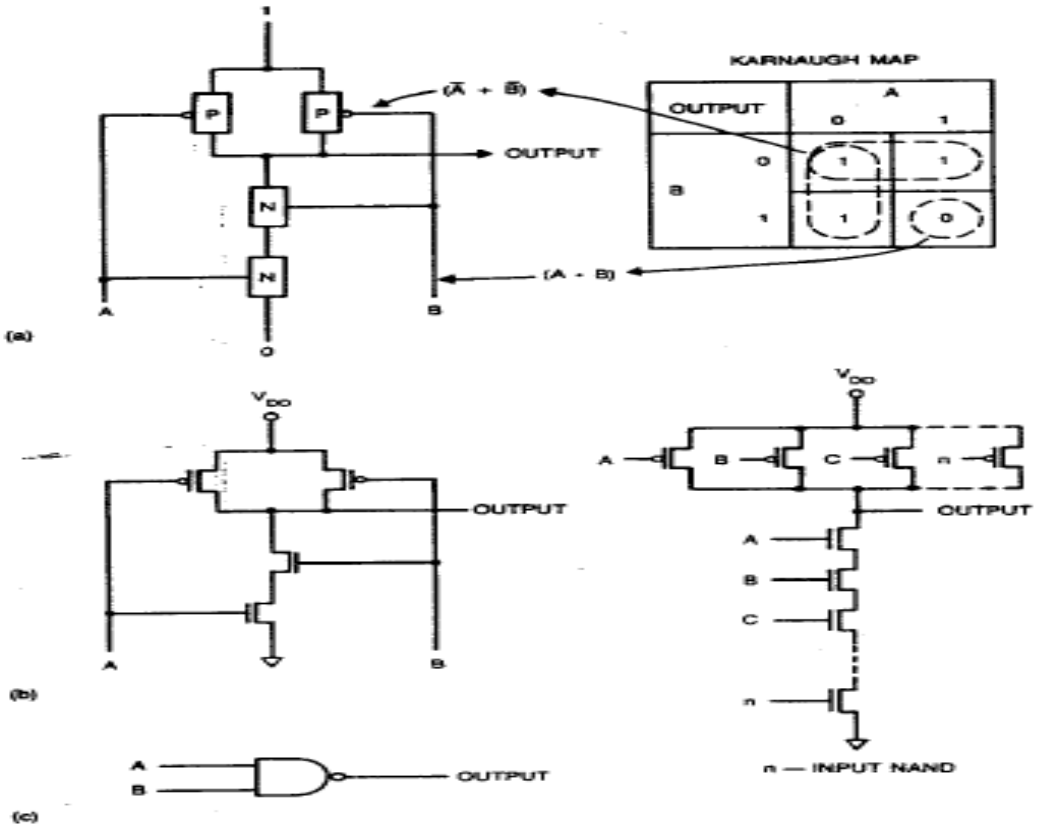


FIGURE 1.6. A CMOS NAND gate

TABLE 1.2. NAND gate truth table

A INPUT	B INPUT	A N-SWITCH	B N-SWITCH	A P-SWITCH	B P-SWITCH	OUTPUT
0	0	OFF	OFF	ON	ON	1
0	1	OFF	ON	ON	OFF	1
1	0	ON	OFF	ON	OFF	1
1	1	ON	ON	OFF	OFF	0

CMOS NOR Gate

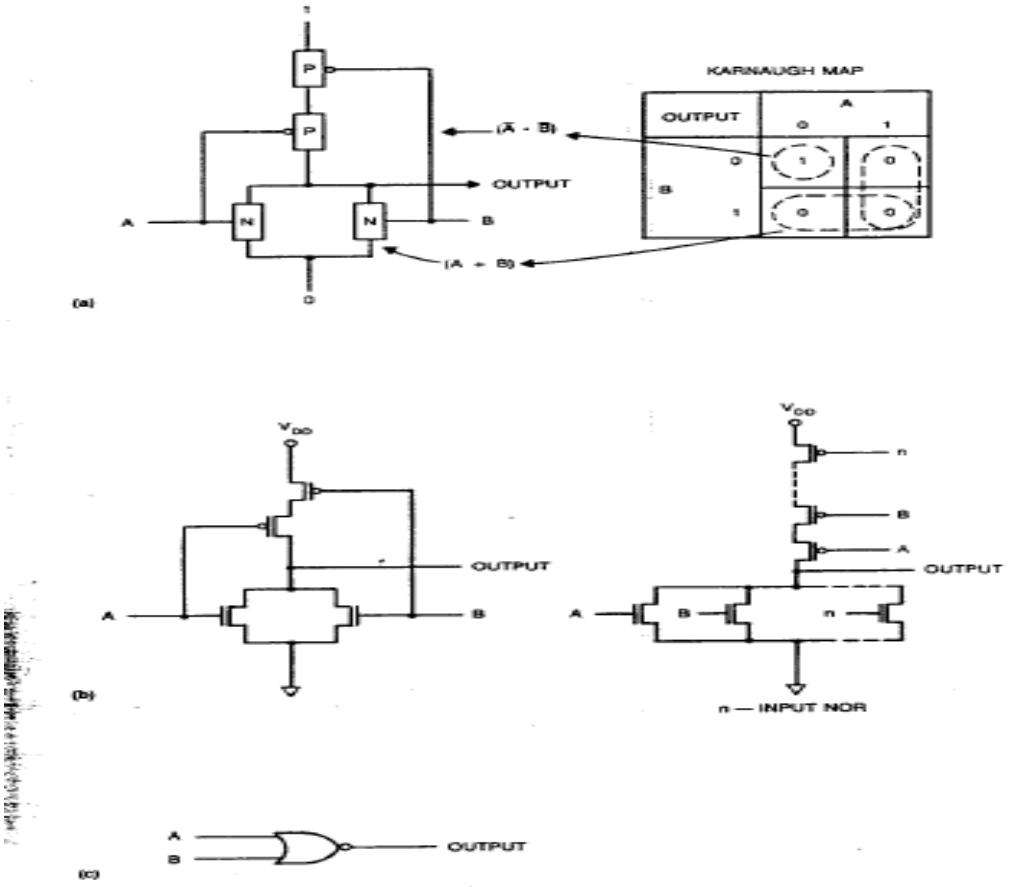
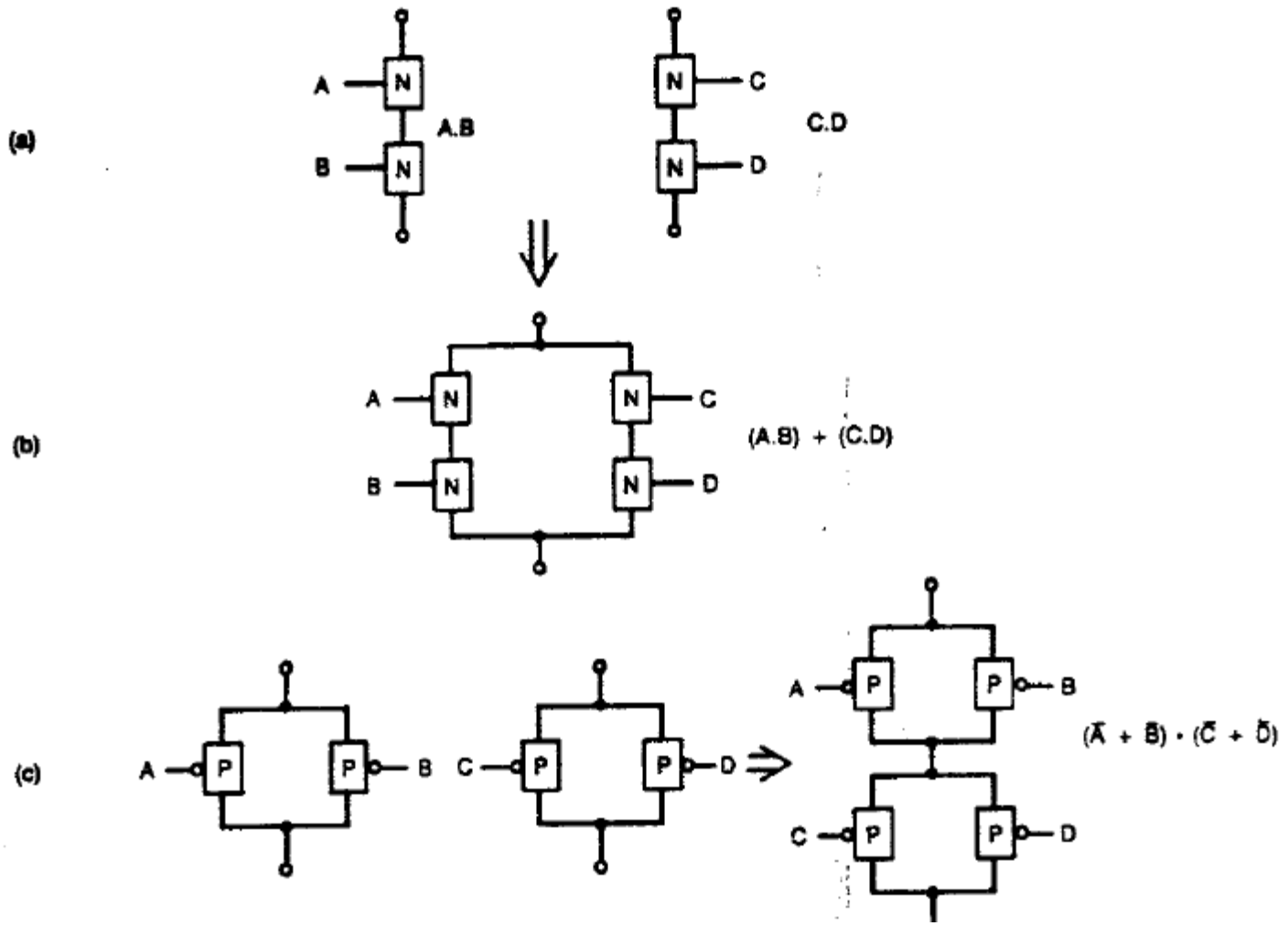


TABLE 1.3. NOR gate truth table

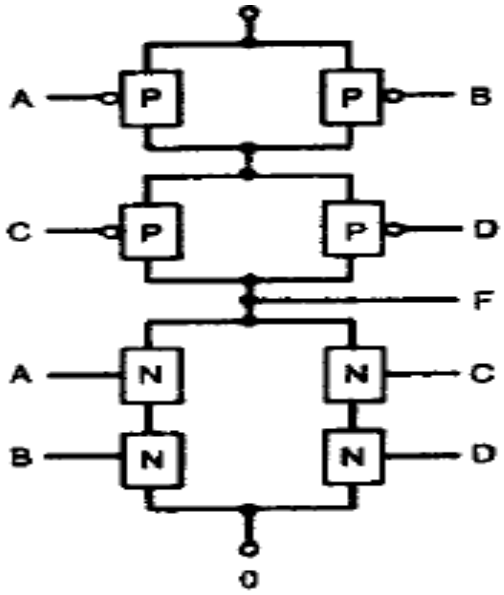
A INPUT	B INPUT	A N-SWITCH	B N-SWITCH	A P-SWITCH	B P-SWITCH	OUTPUT
0	0	OFF	OFF	ON	ON	1
0	1	OFF	ON	ON	OFF	0
1	0	ON	OFF	OFF	ON	0
1	1	ON	ON	OFF	OFF	0

Compound Gates- $F = \overline{((A.B) + (C.D))}$



Contd..

(d)



$$F = \overline{((A \cdot B) + (C \cdot D))}$$

(e)

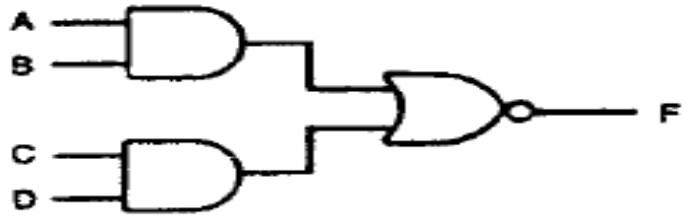


FIGURE 1.8. Construction of function $F = \overline{((A.B) + (C.D))}$

2 to 1 Multiplexer

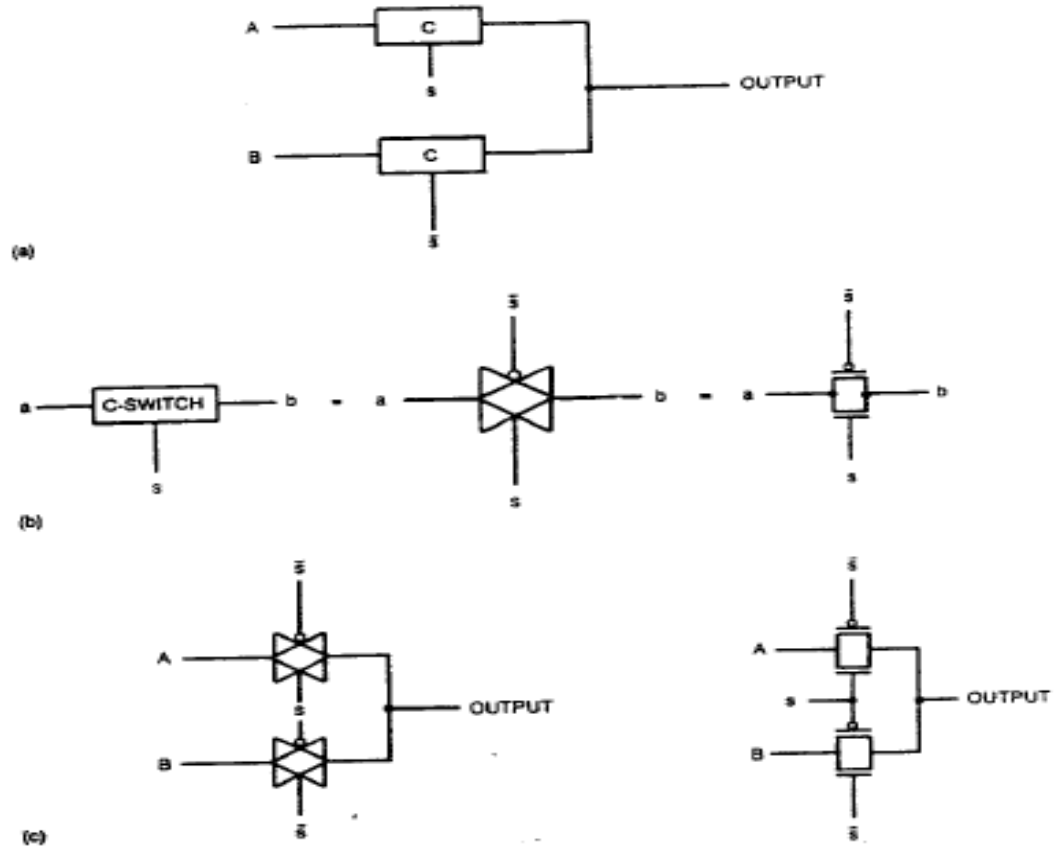
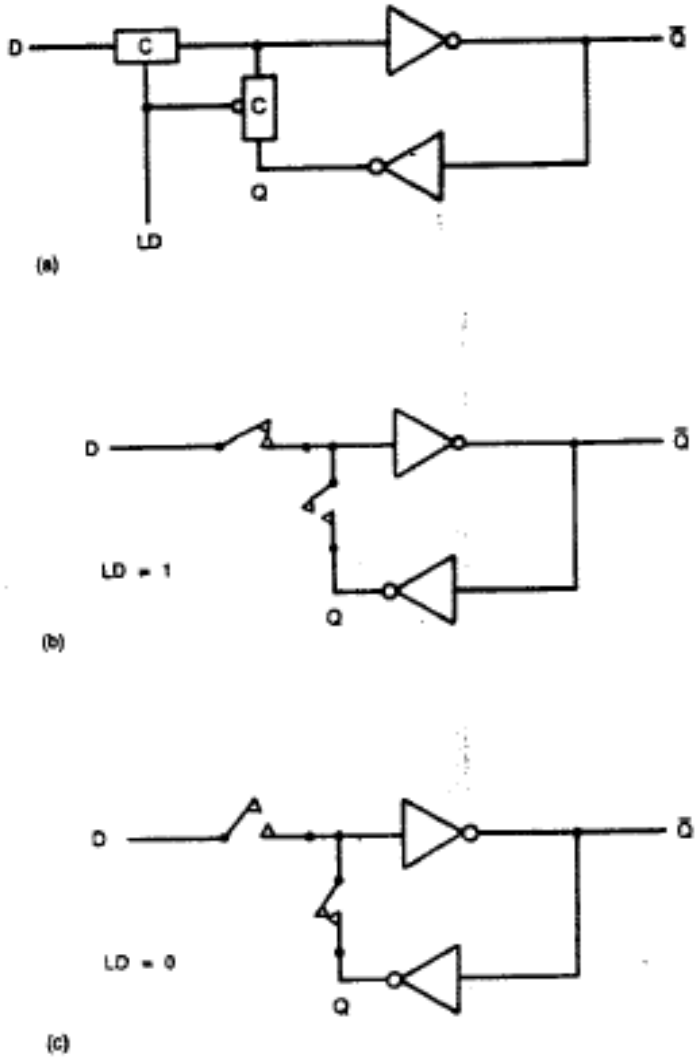


FIGURE 1.10. A CMOS 2-input multiplexer

TABLE 1.4. Two input multiplexer truth table

A	B	S	$\bar{S}$	OUTPUT
X	0	0	1	0(B)
X	1	0	1	1(B)
0	X	1	0	0(A)
1	X	1	0	1(A)

CMOS Flipflop



When LD = '1', $\overline{Q}$ is set to $\overline{D}$ and Q is set to D (Fig. 1.11b). When LD is switched to '0', a feedback path around the inverter pair is established (Fig. 1.11c). This causes the current state of Q to be stored. While LD = '0' the input D is ignored.

Alternate circuit Representation- Behavioral Representation

- $F= \overline{(A+B+C).D}$

- Sum = a + b

- If (LD=1)
- Then
- Q=D;

Alternate circuit Representation-structural Representation-inverter

```
Part   inv  (in)-> out
   Nfet  out  in  vss
   Pfet  out  in  vdd
End
```

Transistor-type	drain-conn	gate-conn	source-conn
Nfet	out	in	vss

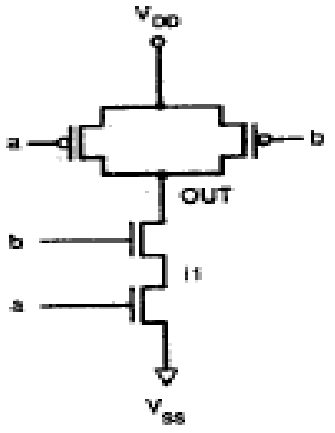
Thus the first statement describes an n-transistor with drain = out, gate = in, source = vss. The second statement describes a p-transistor with drain = out, gate = in, source = vdd.

2 input NAND gate-Behavioral Description

The description for a 2-input NAND gate would be

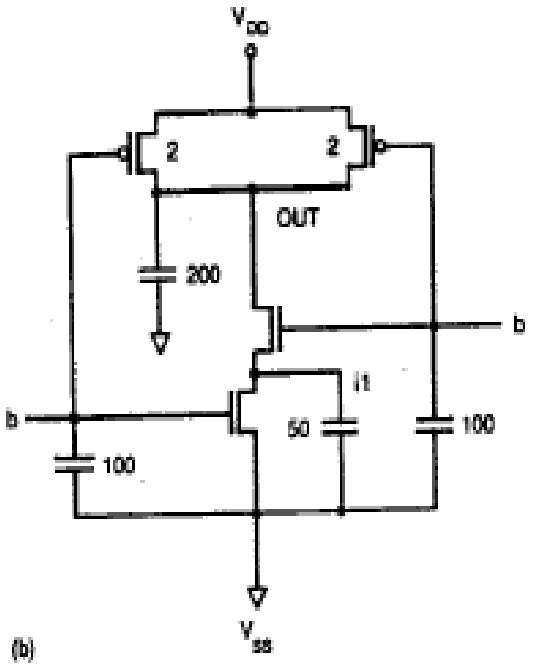
```
Part nand2 (a,b) -> out
Signal il
     Nfet il a vss
     Nfet out b il
     Pfet out a vdd
     Pfet out b vdd
End
```

```
out = -(a&b)
```



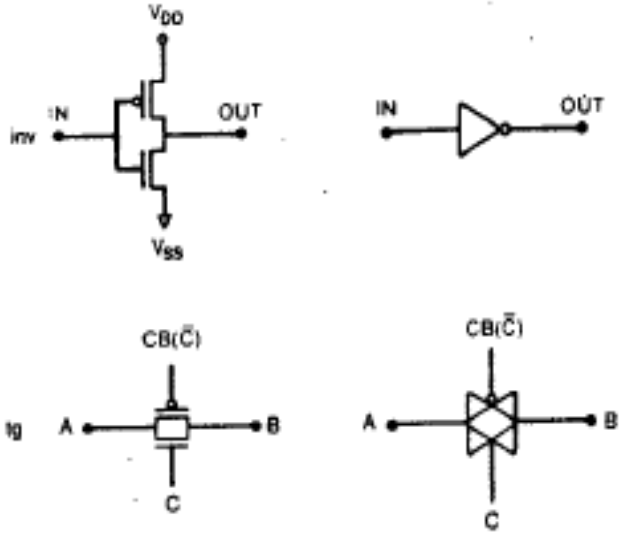
2 input NAND gate-Structural Description

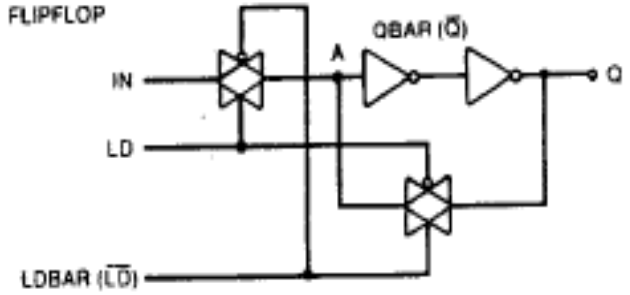
```
Part nand2 (a,b) -> out
Signal i1
      Nfet  i1 a vss
      Nfet out b i1
      Pfet out a vdd size = 2
      Pfet out b vdd size = 2
      Capacitance i1 50
      Capacitance  a 100
      Capacitance  b 100
      Capacitance out 200
End
```



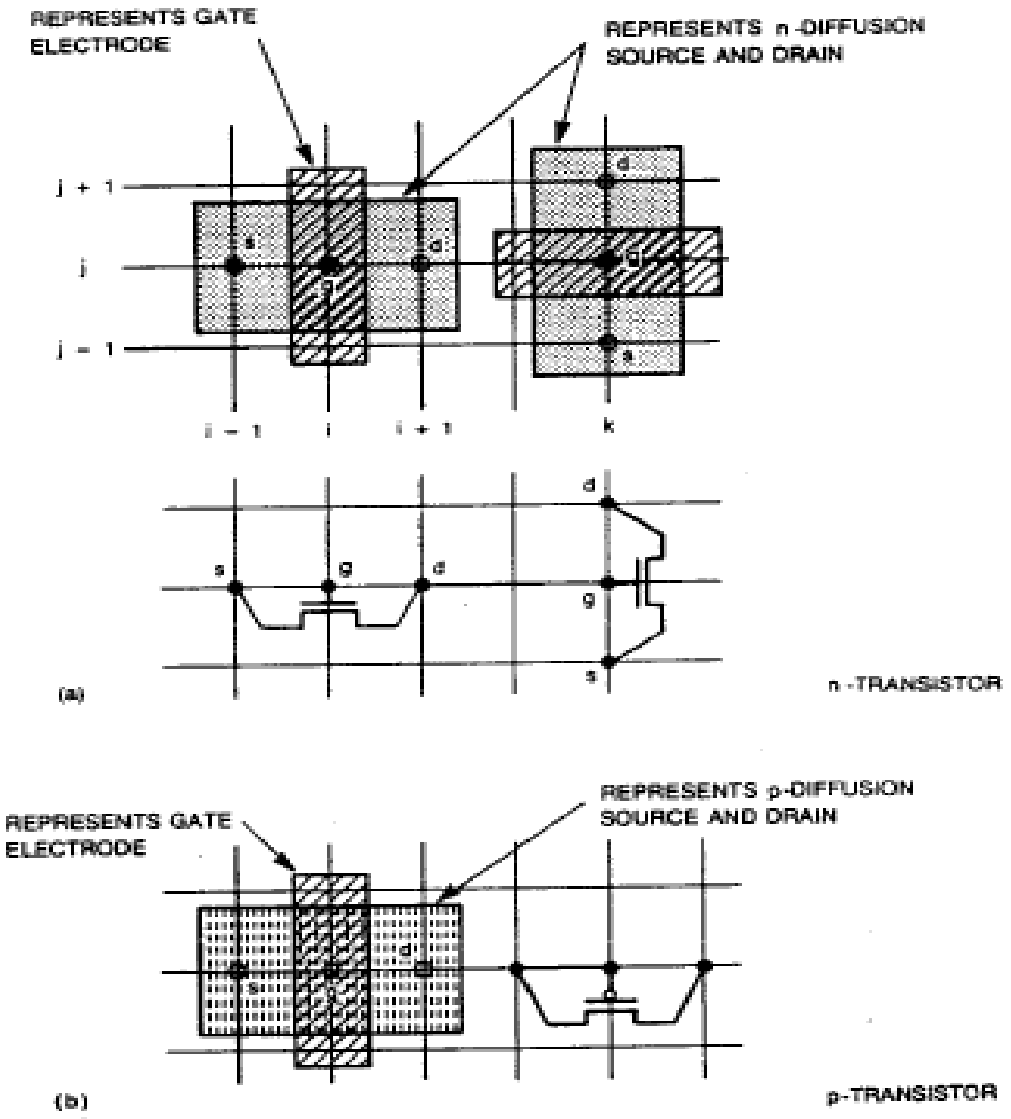
Flipflop

```
Part flipflop (in, ld, ldbar, q, qbar)
Signal a
       tg (in, ld, ldbar) -> a
       inv (a) -> qbar
       inv (qbar) -> q
       tg (q, ldbar, ld) -> a
End
```

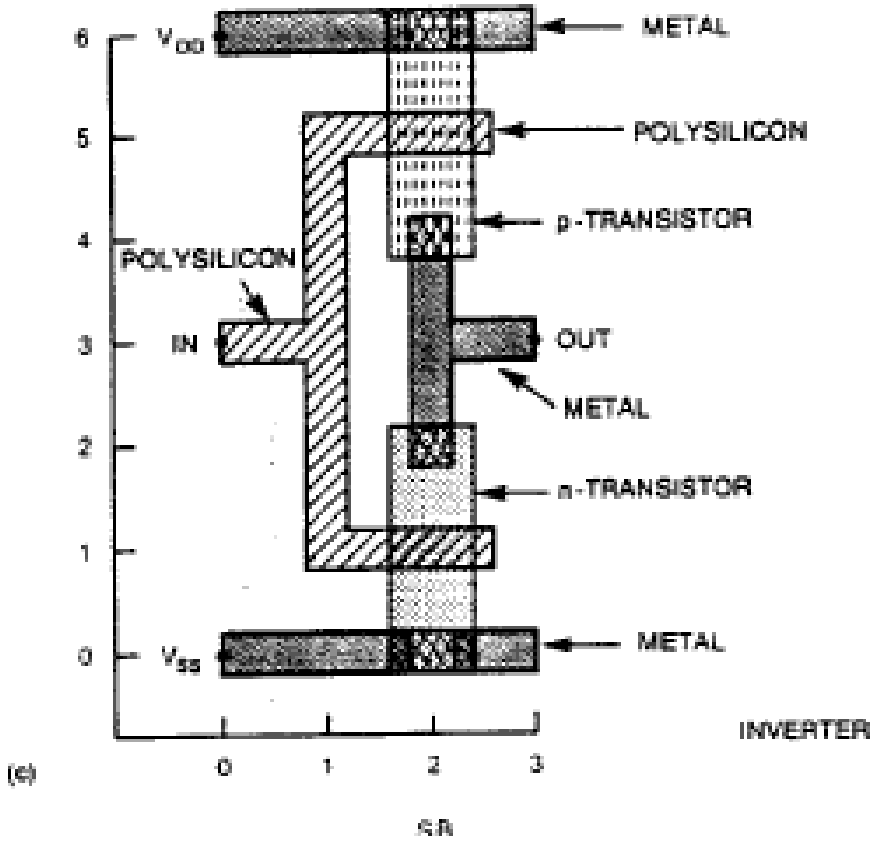




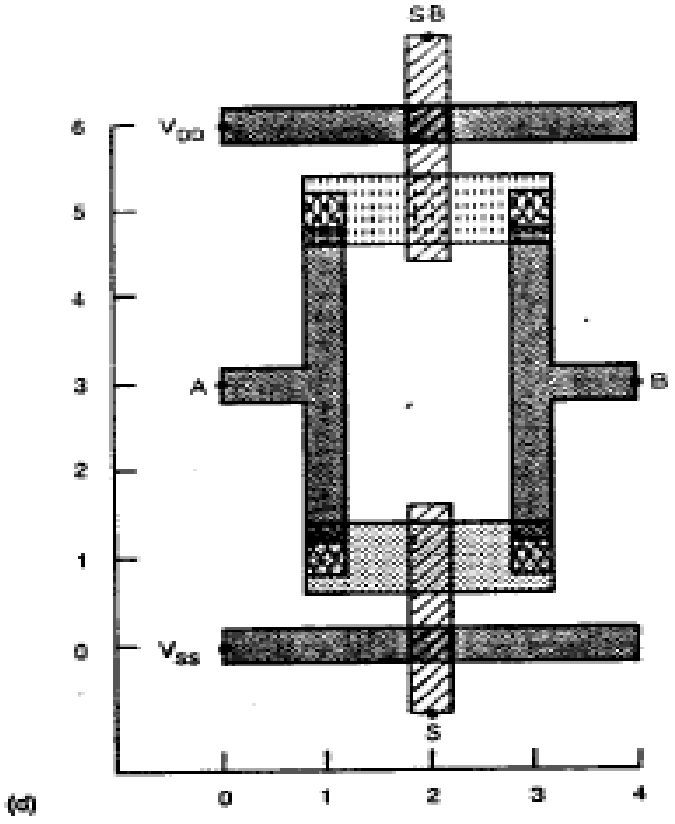
Physical Representation-NMOS &PMOS



Physical Representation-Inverter



Physical Representation-Transmission Gate



TRANSMISSION GATE

CMOS V/S NMOS

- **Comparison:**

Feature	CMOS (Complementary)	NMOS (Single Type)
Power Consumption	Low (except during switching)	Higher (due to static current flow)
Speed	High (due to low capacitance)	High (but can be slower in certain configurations)
Logic Implementation	More flexible, used in large-scale designs	Simple but less efficient
Drive Current	Better (due to use of both PMOS and NMOS)	Limited (only one type of transistor)